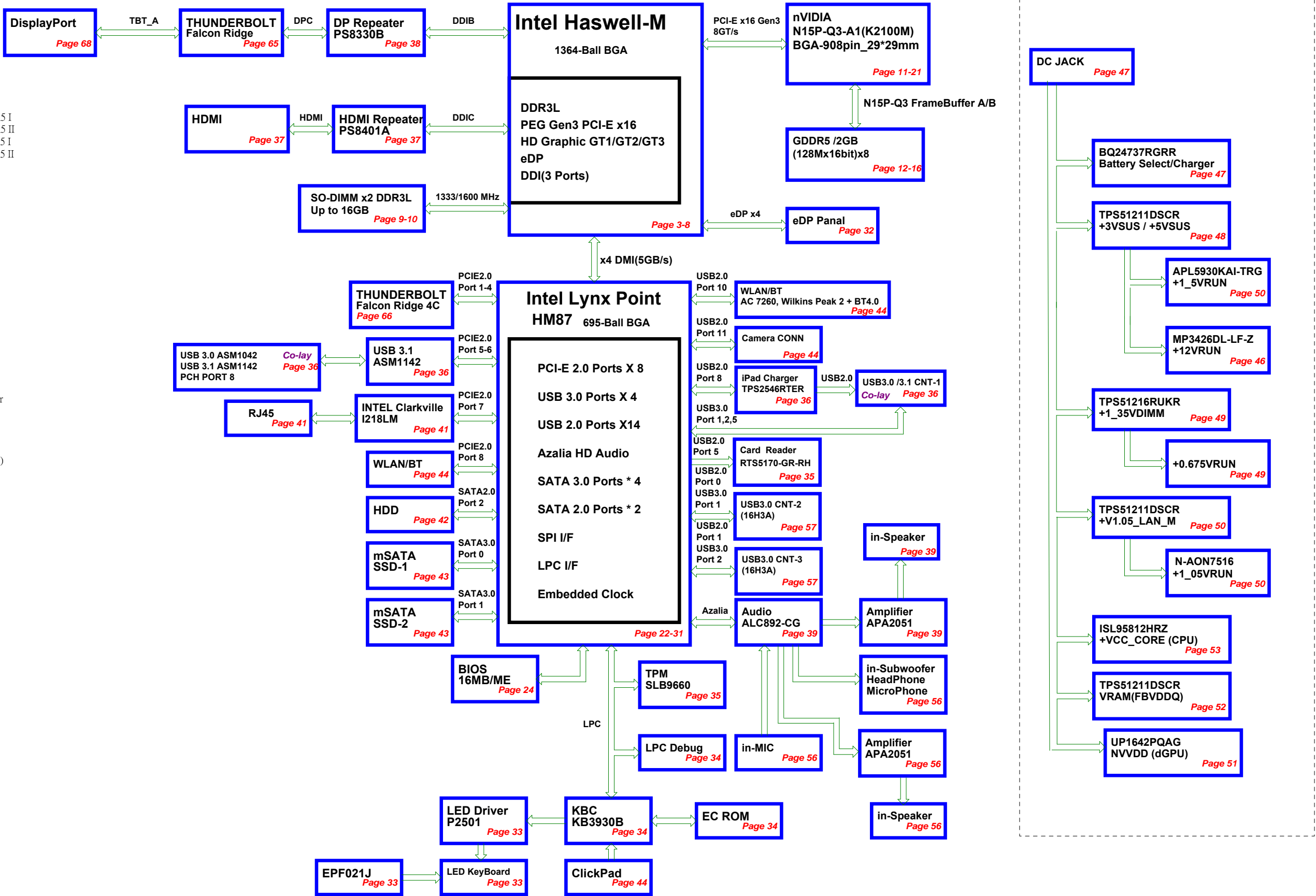


Shark Bay Mobile

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

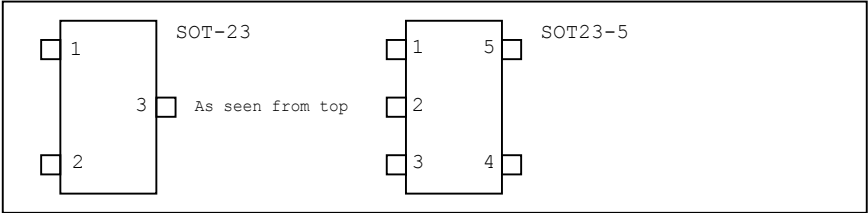
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx = Like Test Point, but using VIA.

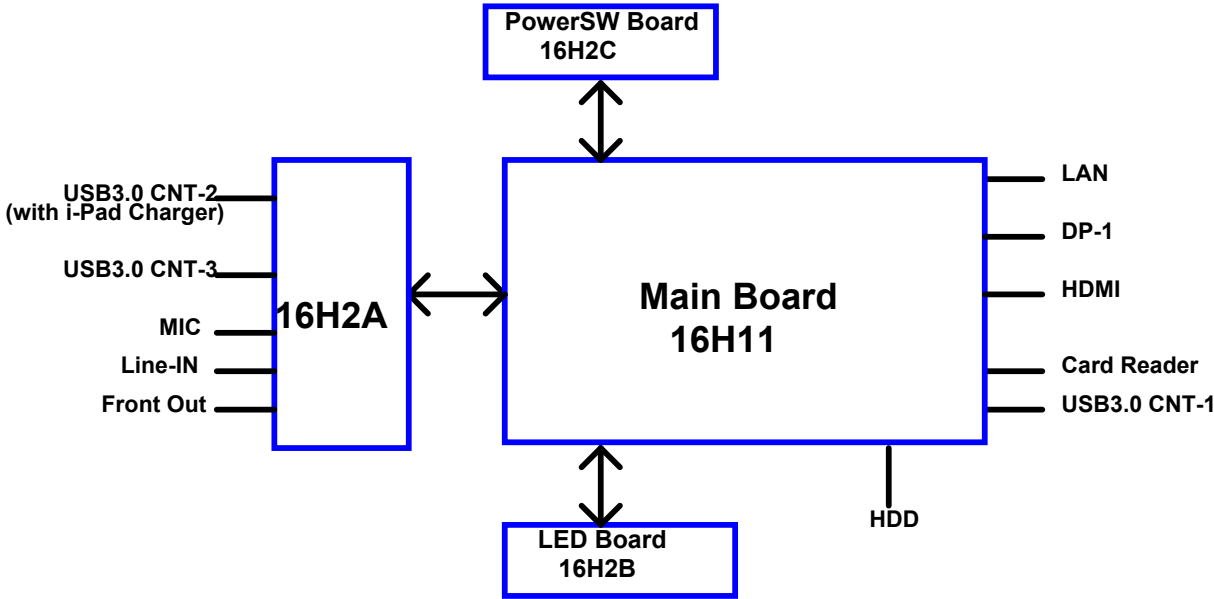
PCB Footprints



POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high



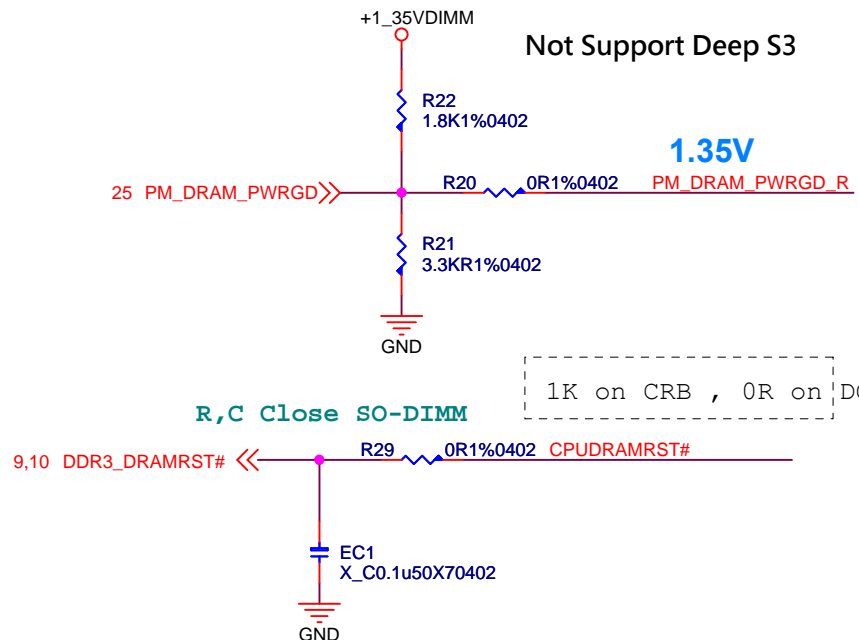
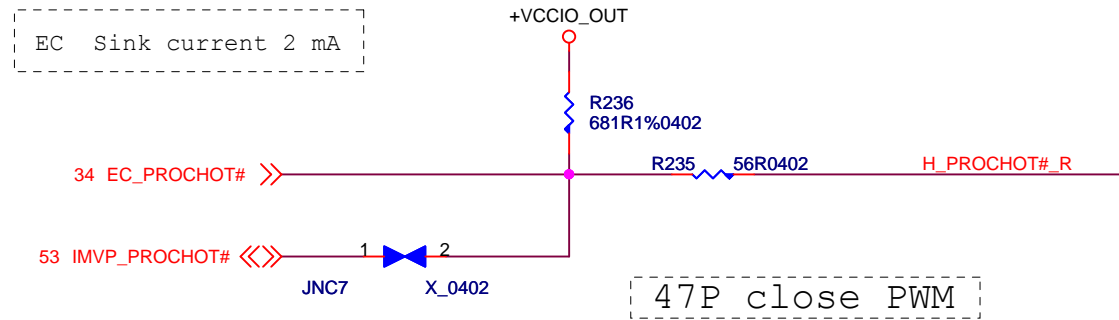
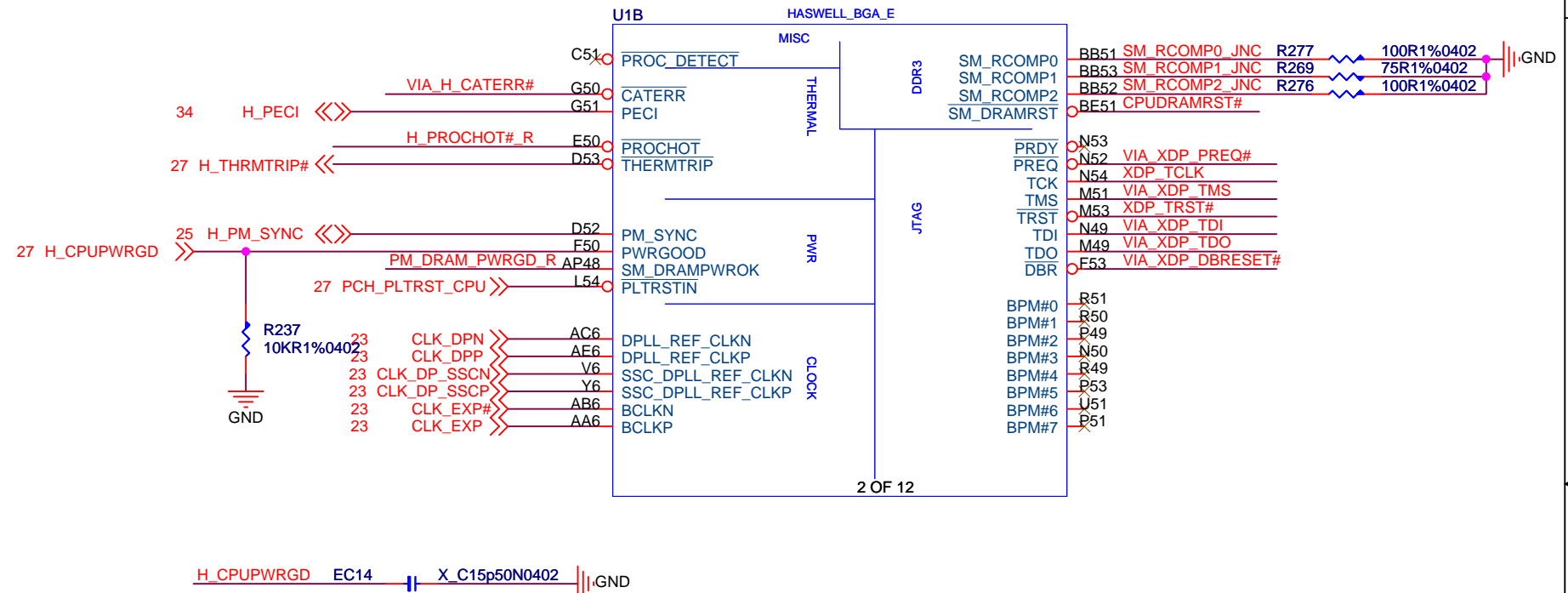
Haswell (DMI,PEG,FDI)

PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

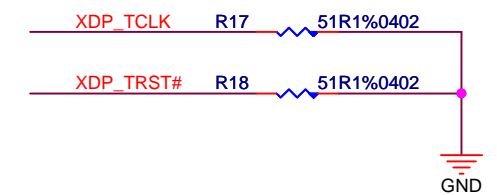


Haswell (CLK,MISC,JTAG)

SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil

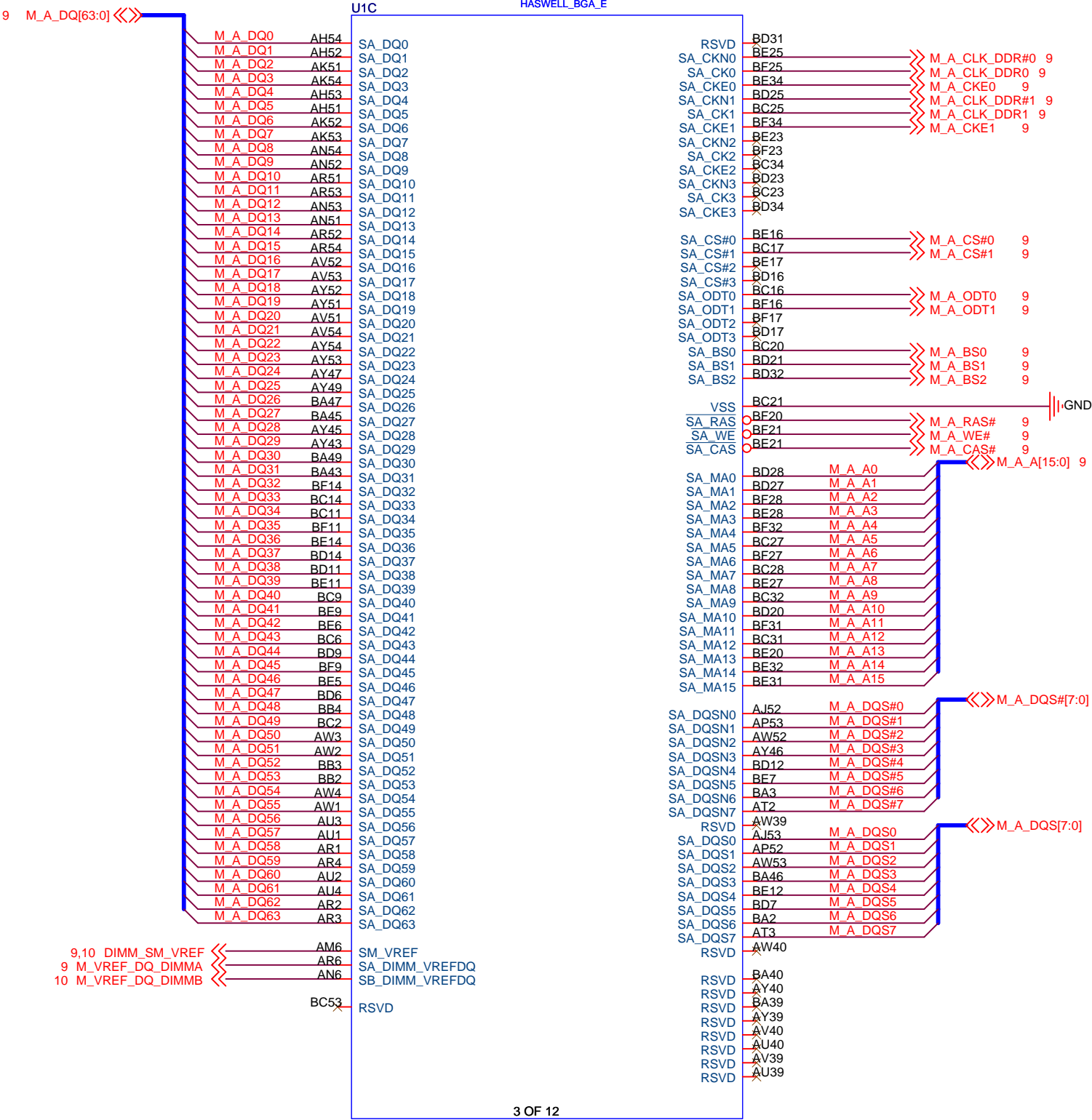


p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.

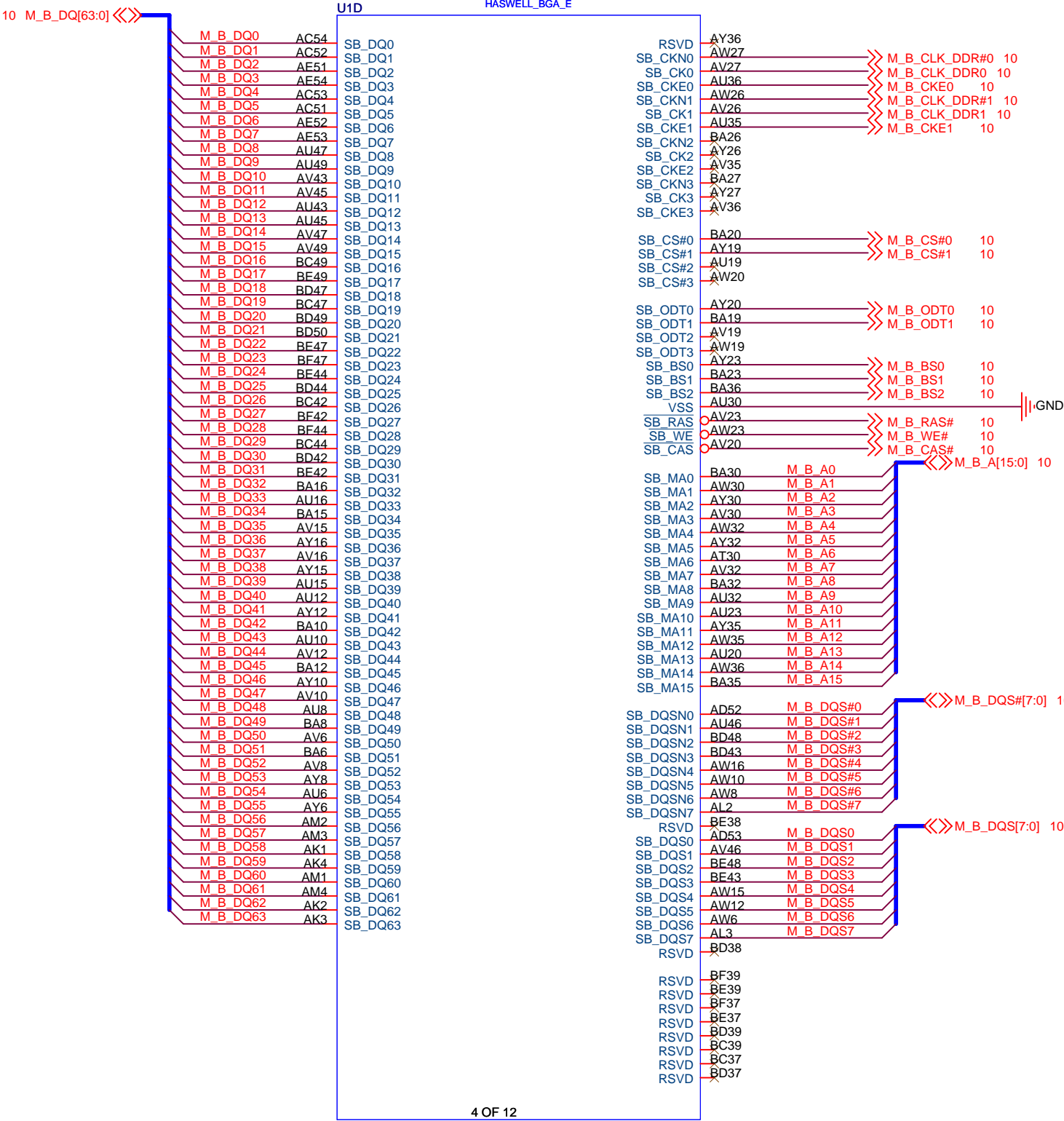


Haswell (DDR3L)

SODIMM#A



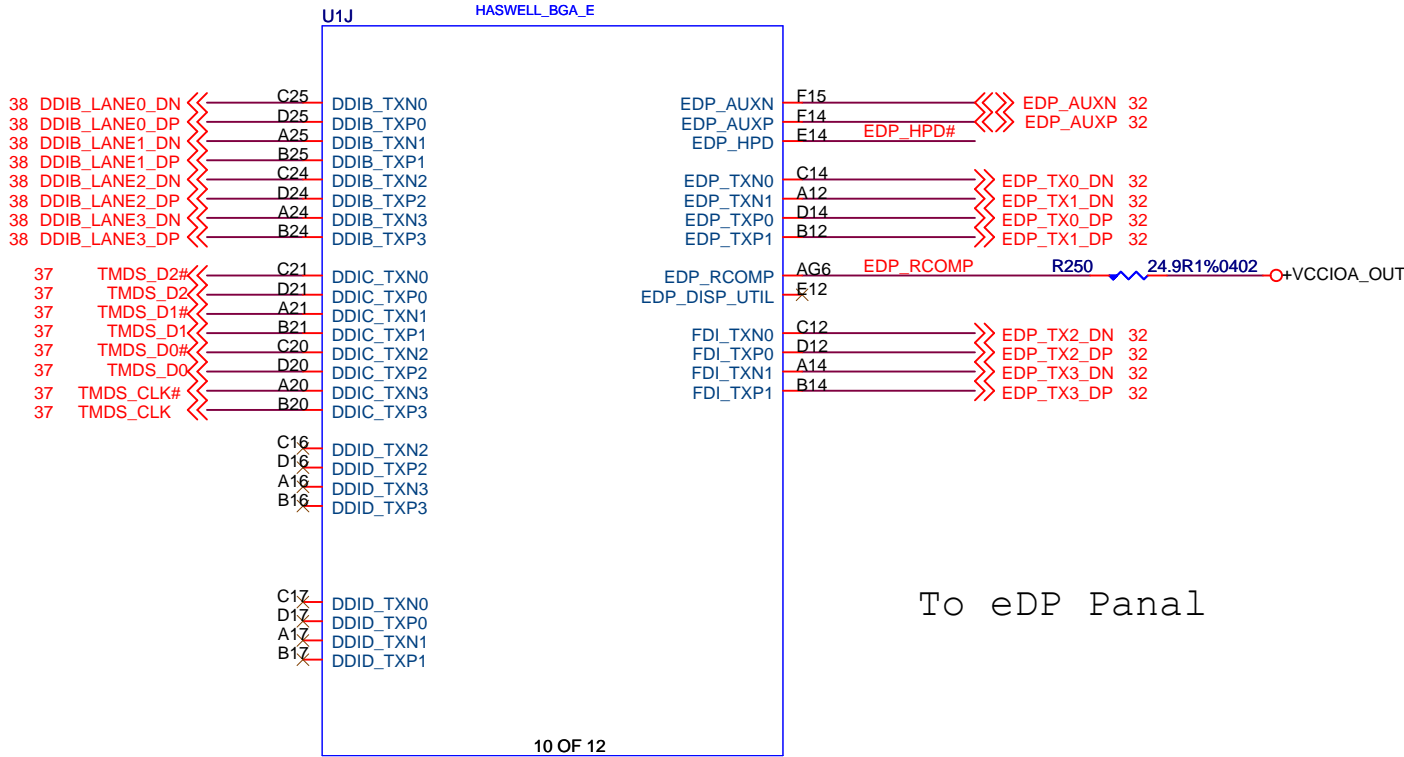
SODIMM#B



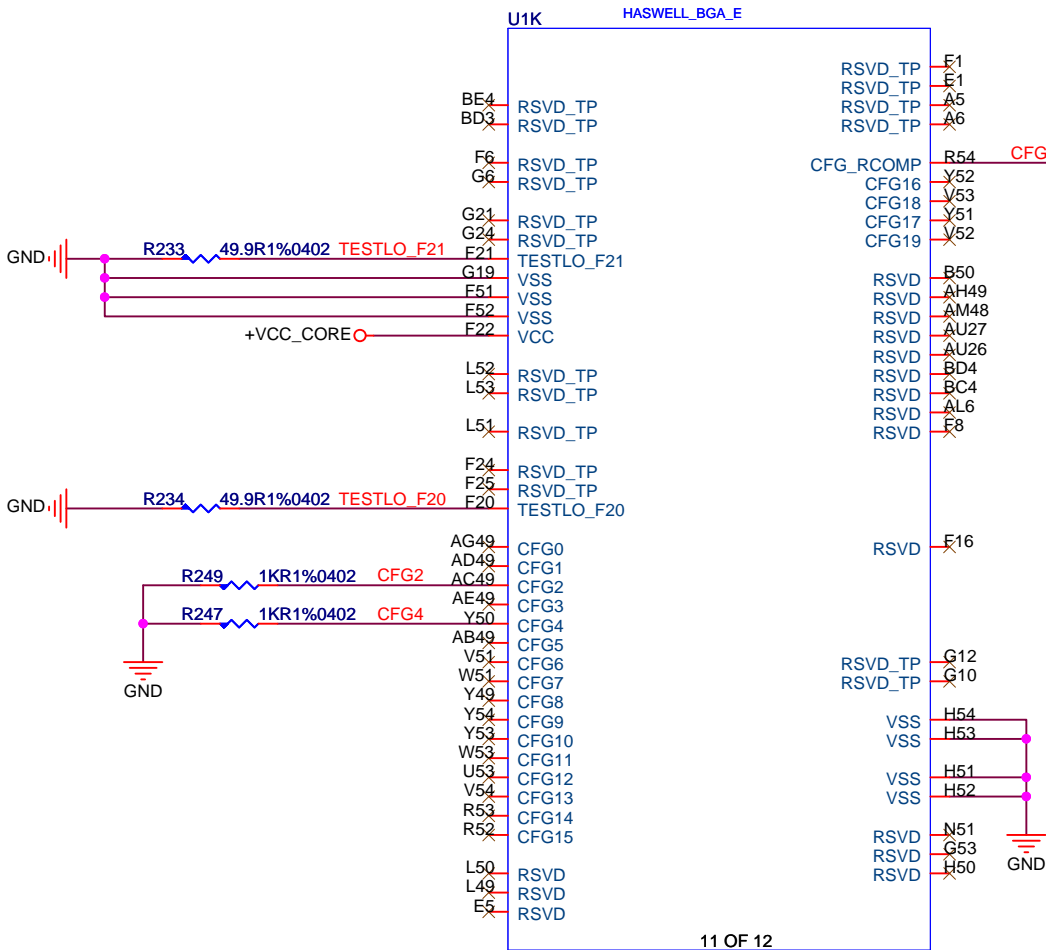
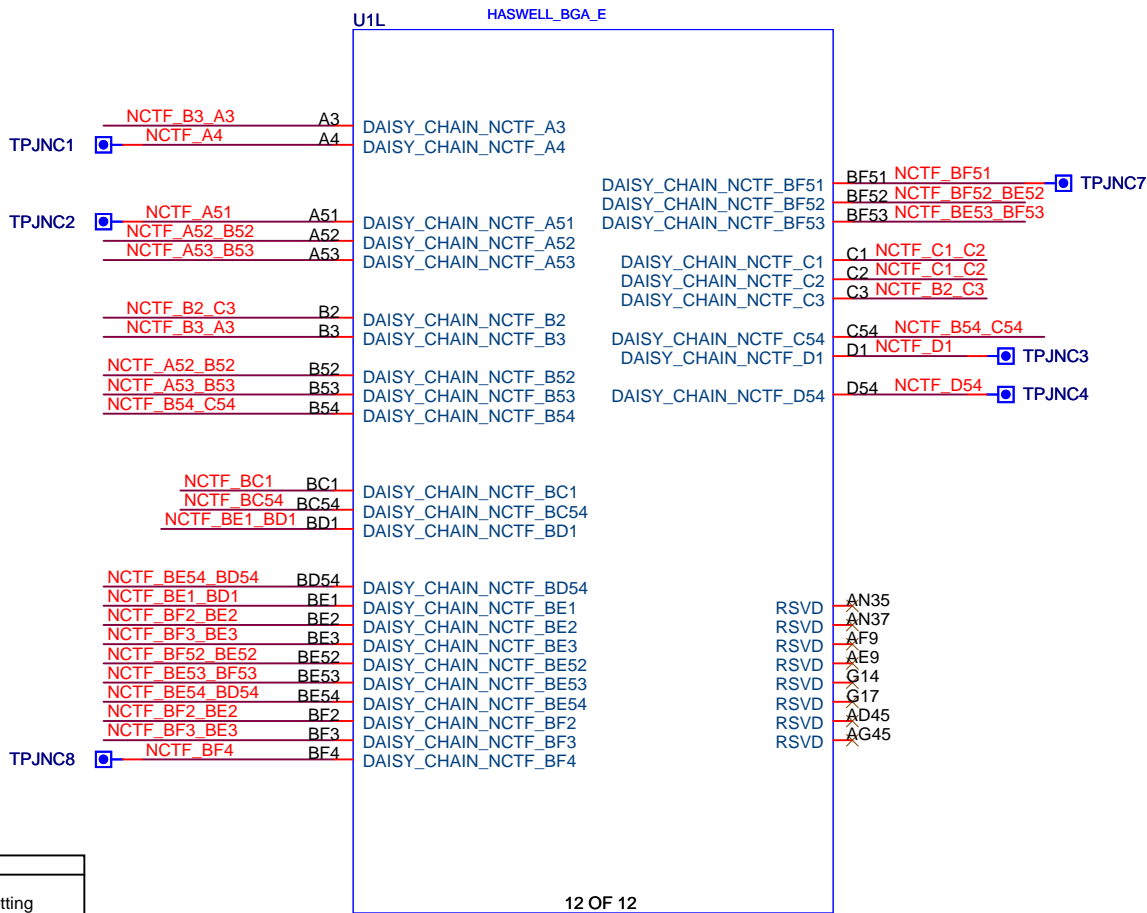
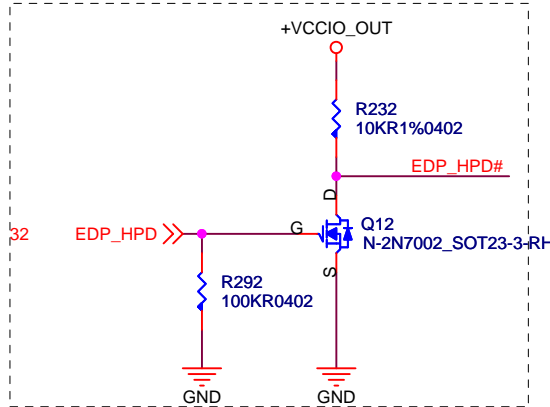
Display/Reserved

DP

HDMI



To eDP Panel



PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

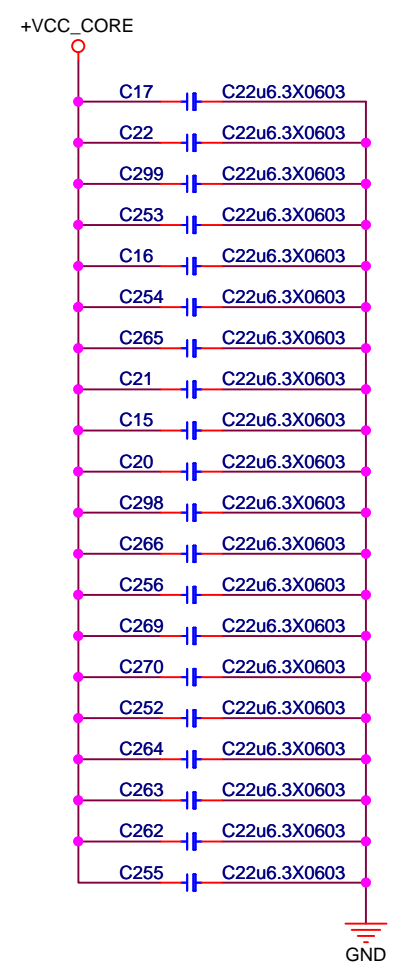
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

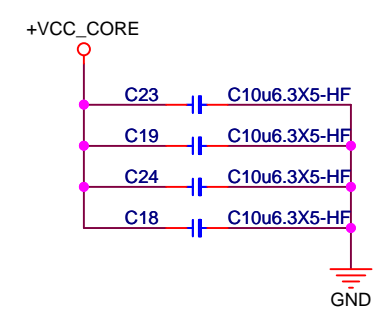
PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

22uF x 20 /0603
C11-2267313-T04

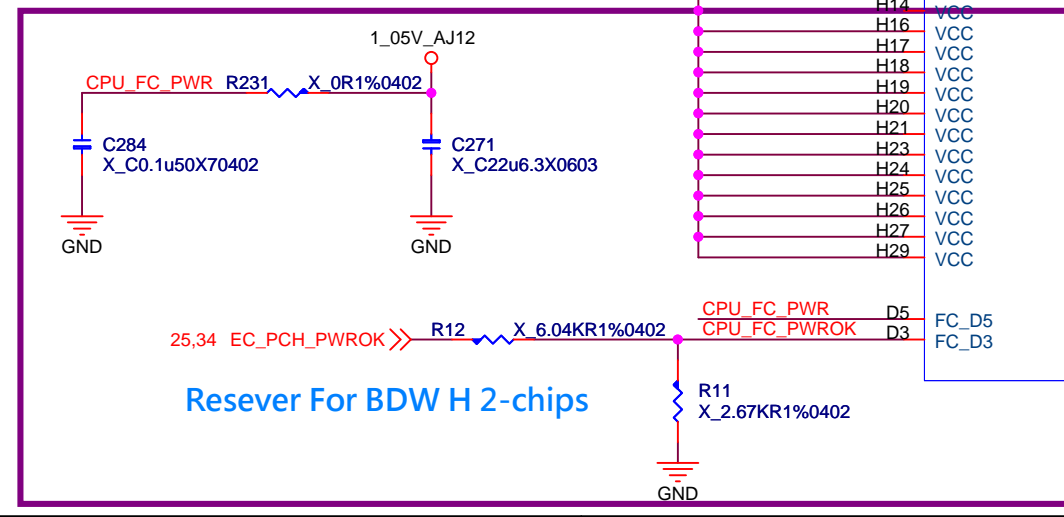


10uF x 4 /0603
C11-1067333-Y01



	Haswell	Boardwell
R231	No Stuff	Stuff
C284	No Stuff	Stuff
C271	No Stuff	Stuff
R12	No Stuff	Stuff
R11	No Stuff	Stuff

2014.2.20 Modify for Haswell CPU



Haswell (POWER)

+VCC_CORE

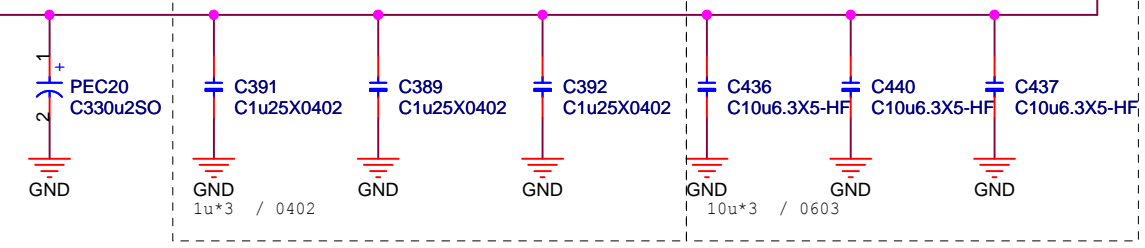
95A

HASWELL_BGA_E

U1E

- RSVD J17
- RSVD J21
- RSVD J26
- RSVD J31
- VDDQ AR29
- VDDQ AR31
- VDDQ AR33
- VDDQ AT13
- VDDQ AT19
- VDDQ AT23
- VDDQ AT27
- VDDQ AT32
- VDDQ AT36
- VDDQ AV37
- VDDQ AW22
- VDDQ AW25
- VDDQ AW29
- VDDQ AW33
- VDDQ AY18
- VDDQ BB21
- VDDQ BB22
- VDDQ BB26
- VDDQ BB27
- VDDQ BB30
- VDDQ BB31
- VDDQ BB34
- VDDQ BB36
- VDDQ BD22
- VDDQ BD26
- VDDQ BD30
- VDDQ BD33
- VDDQ BE18
- VDDQ BE22
- VDDQ BE26
- VDDQ BE30
- VDDQ BE33
- RSVD AN31
- VCC L6
- VCC M6
- RSVD AN22
- RSVD AN18
- VCC_SENSE C50
- RSVD AH9
- VCCIO_OUT D51
- FC_F17 F17
- VCOMP_OUT AK6
- RSVD AN33
- RSVD W9
- RSVD J12
- RSVD AR49
- VIDALERT J53
- VIDSCLK J52
- VIDSOUT J50
- VSS B51
- PWR_DEBUG E19
- VSS E52
- RSVD_TP Y49
- RSVD_TP U49
- RSVD_TP AM49
- RSVD_TP W49
- VSS V50
- VSS AN49
- VSS AJ49
- VSS AG50
- VSS AK49
- VSS AJ50
- VSS AP49
- VSS AB50
- VSS AP50
- VSS AD50
- VSS AM50
- VCC A36
- VCC A38
- VCC A39
- VCC A42
- VCC A43
- VCC A45
- VCC A46
- VCC A48
- VCC AA46
- VCC AA47
- VCC AA8
- VCC AA9
- VCC VCC

4.2 A



+VCC_CORE

	Haswell	Boardwell
R229	No Stuff	Stuff

300 mA

VCCSENSE 53

FC_F17

VCCIOA_OUT

2014.2.20 Modify for Haswell CPU

VR_SVID_ALERT# R

VR_SVID_CLK

VR_SVID_DATA

PWR_DEBUG#

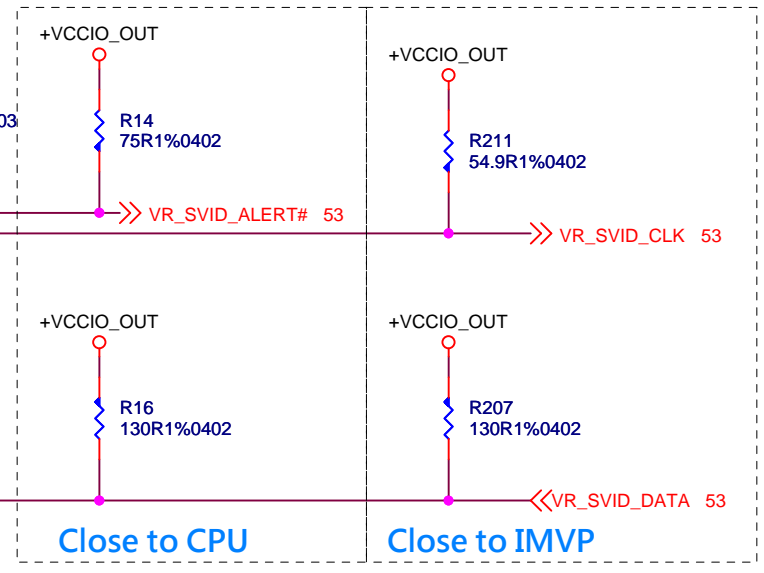
VIA_IVR_ERROR

VIA_IJT_TRIGGER

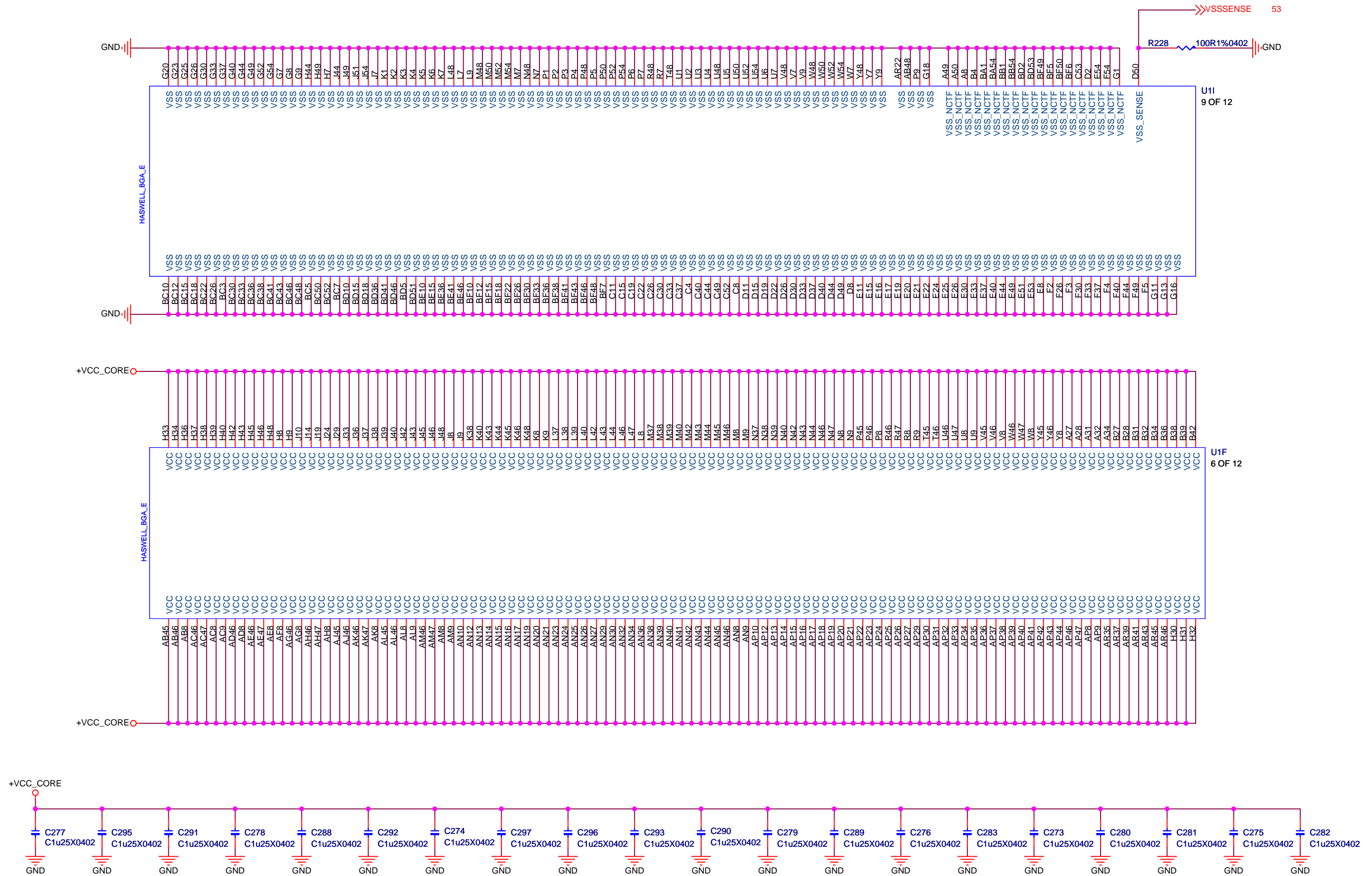
If XDP not implemented, then Route Processor PWR_DEBUG as a test point. This Test point must be clearly labeled

5 OF 12

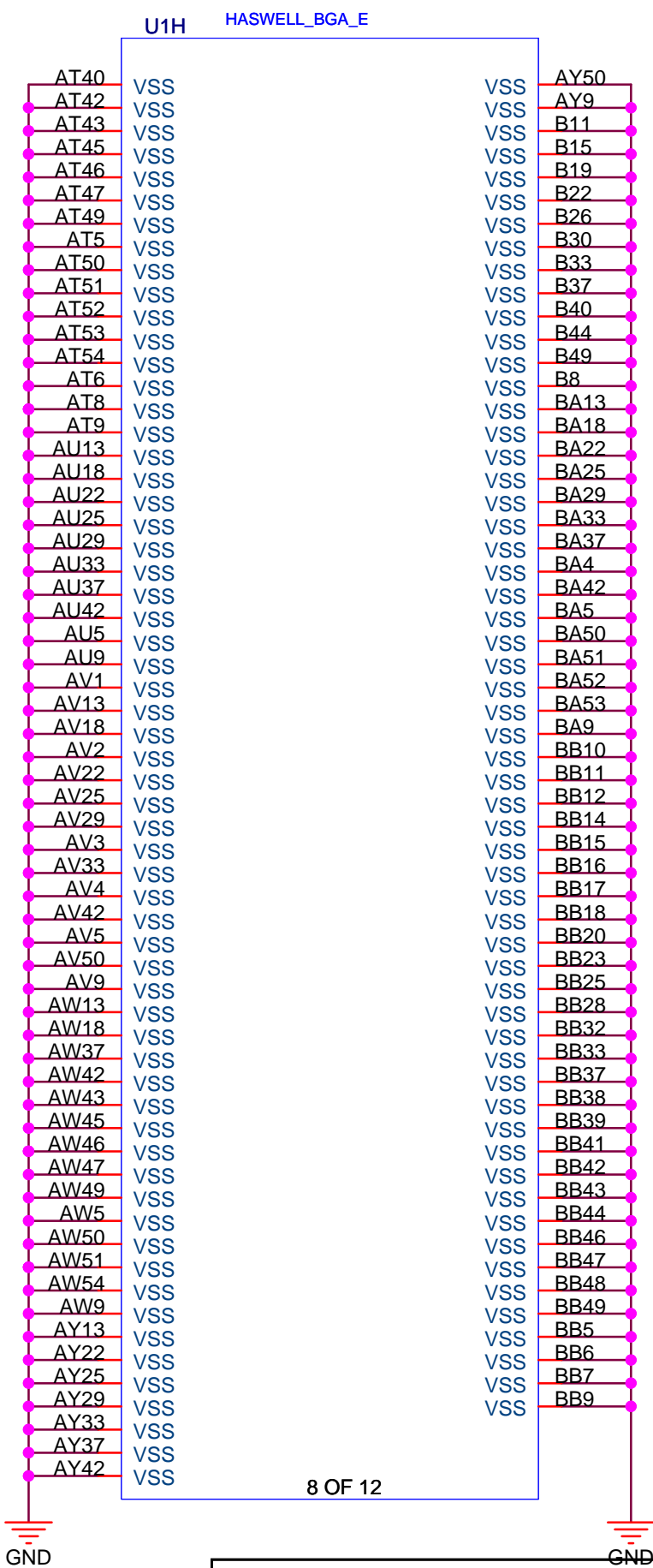
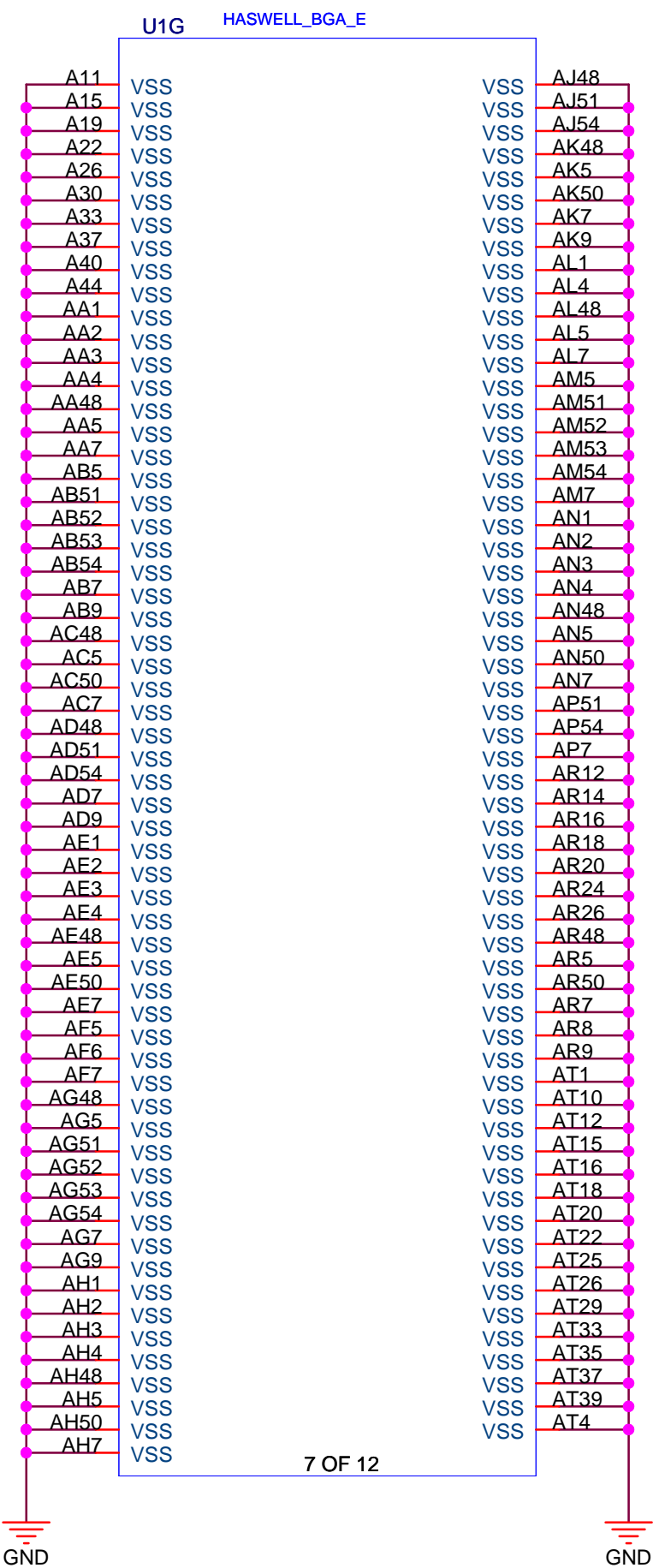
CLK and DATA Misatch 2000mils
SVID total Length not over 6"



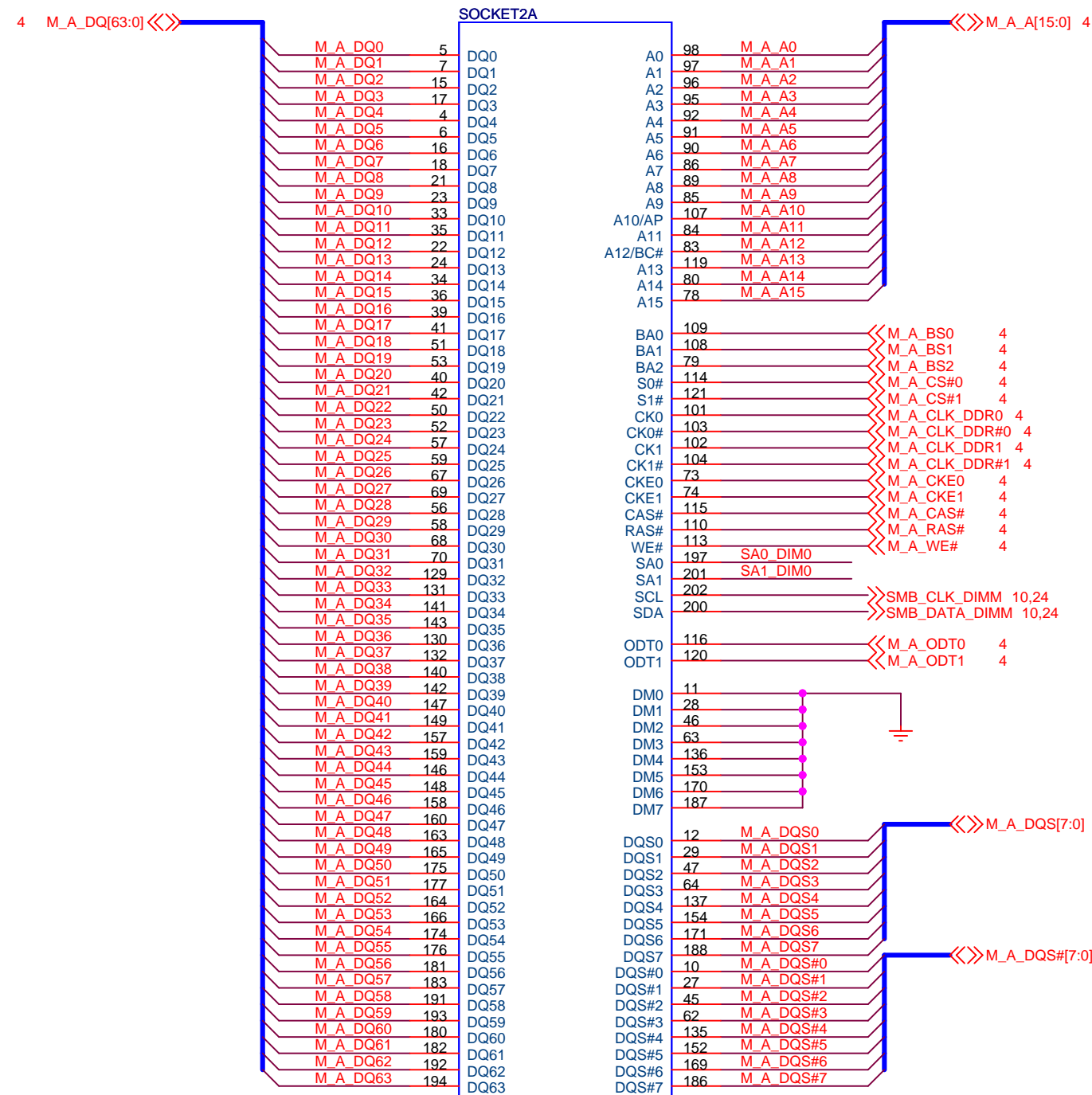
Haswell (Power & GND)



Haswell (GND)

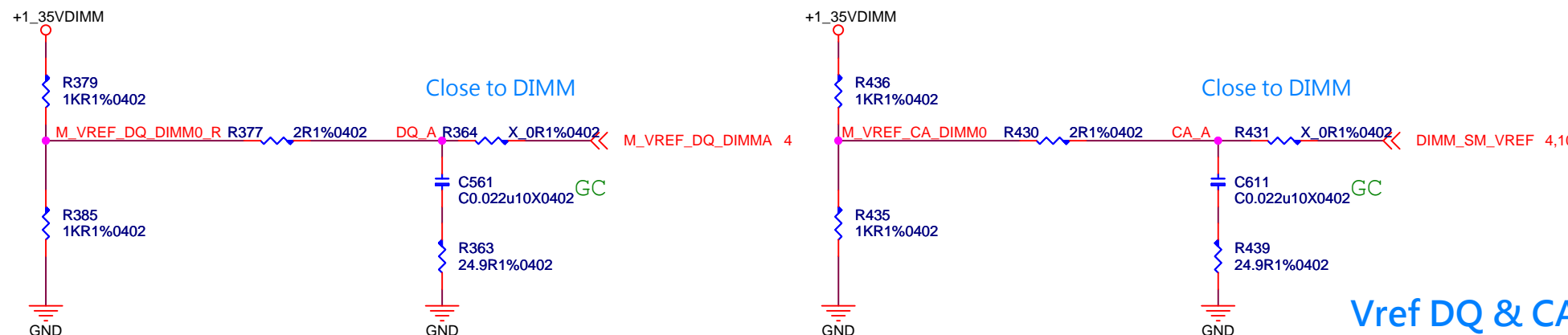
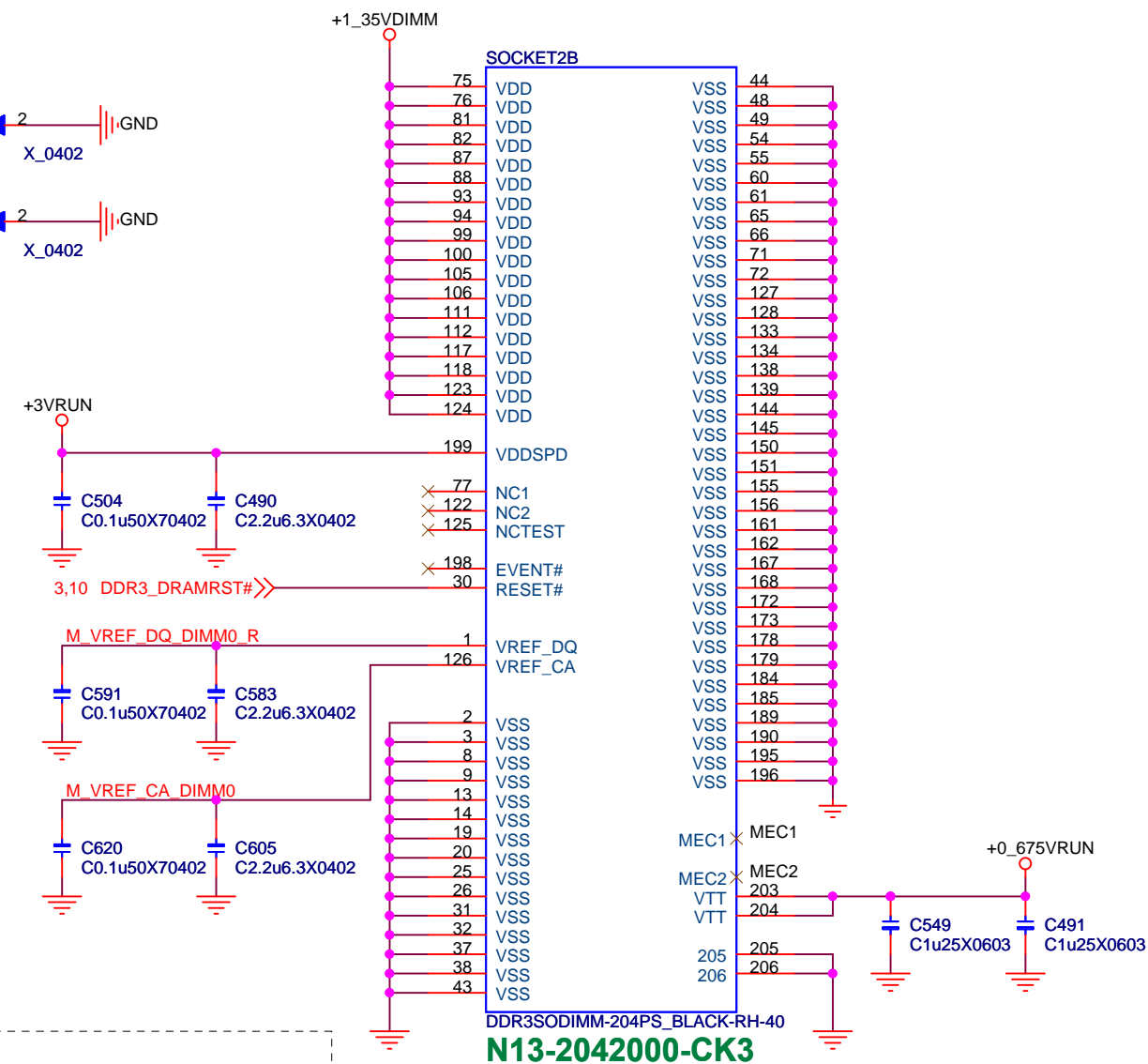
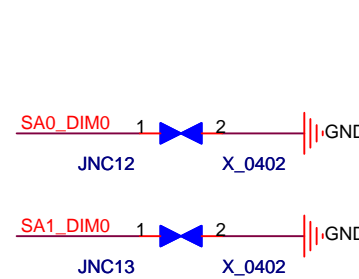
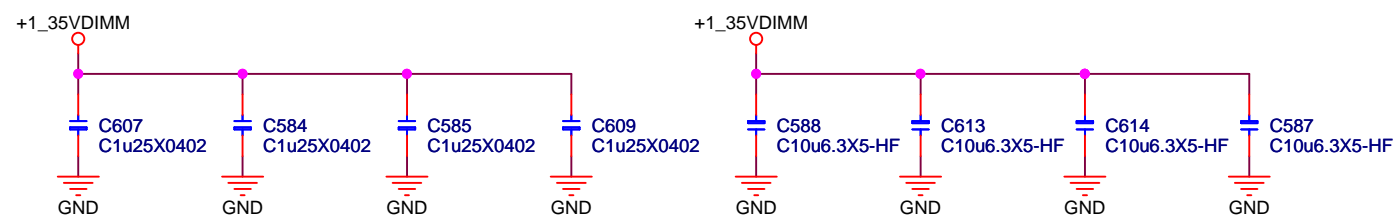


SODIMM#A

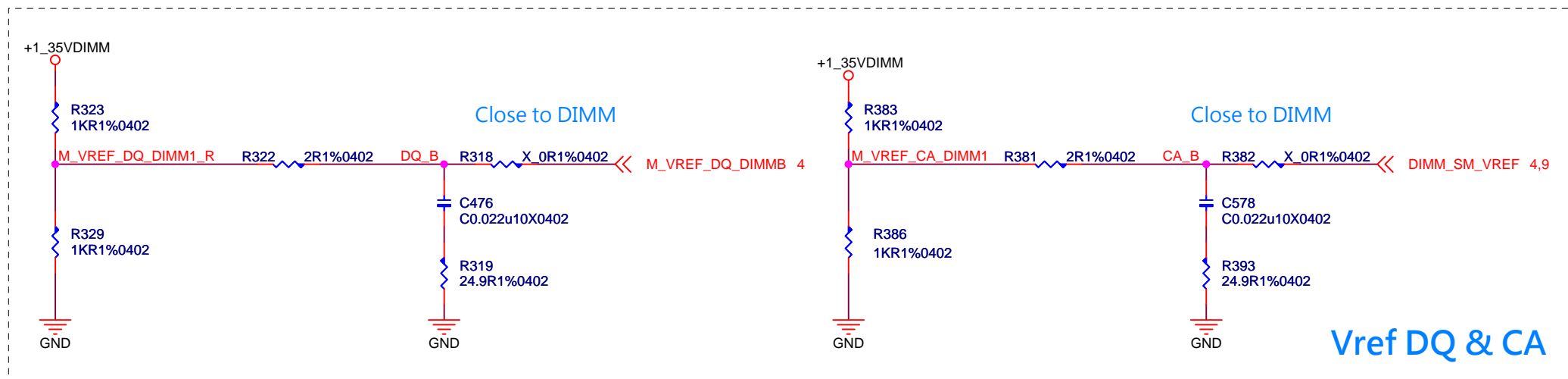
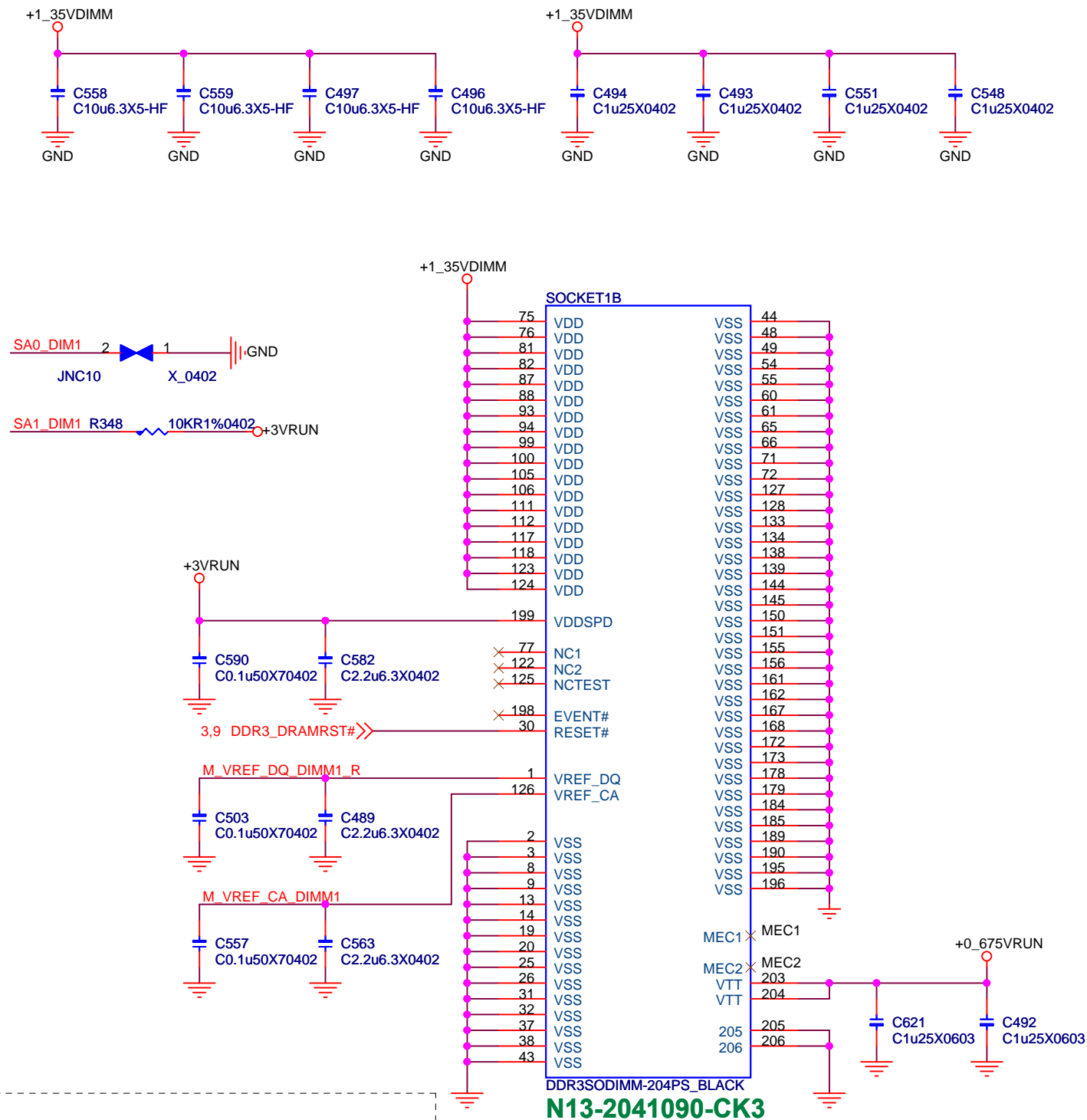
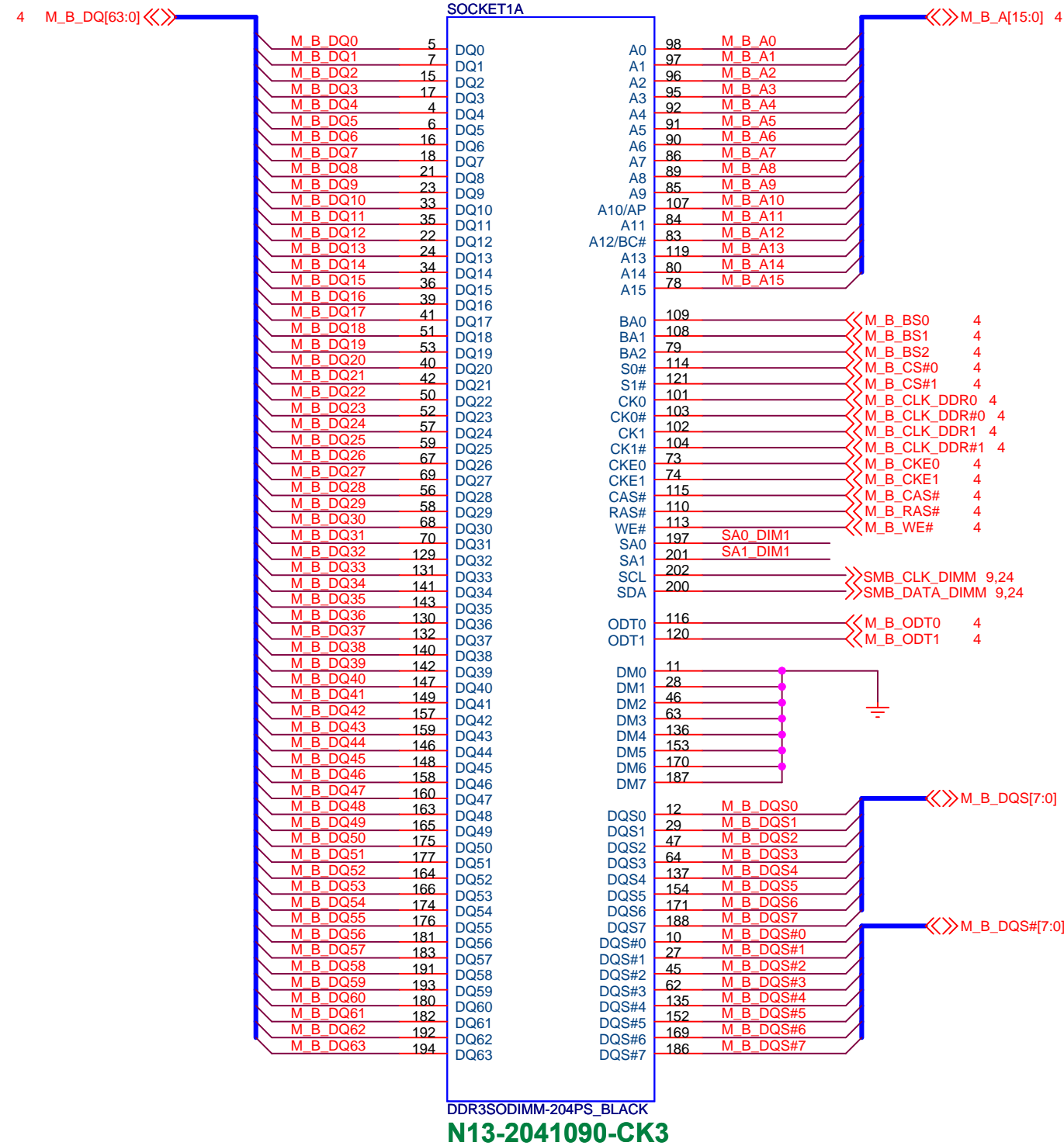


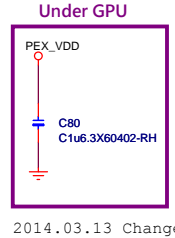
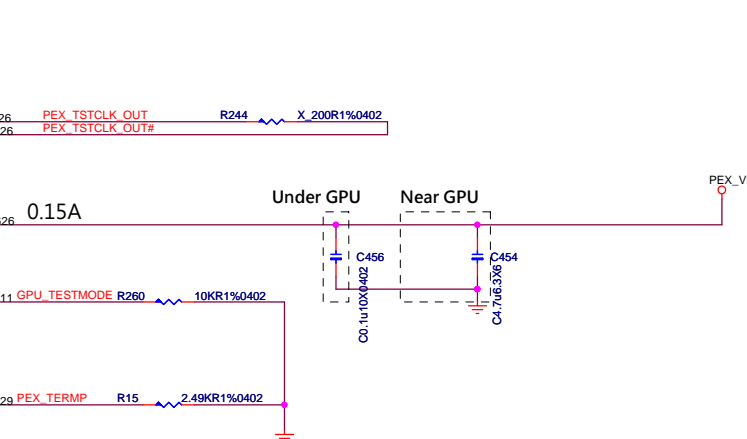
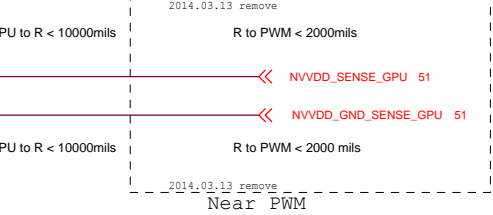
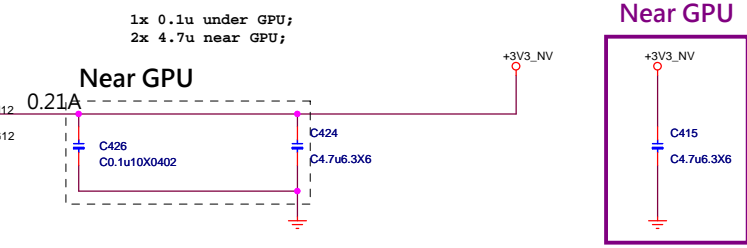
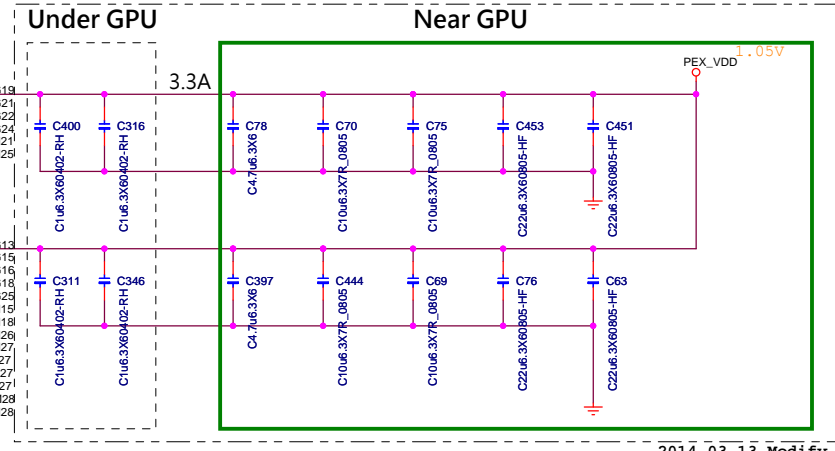
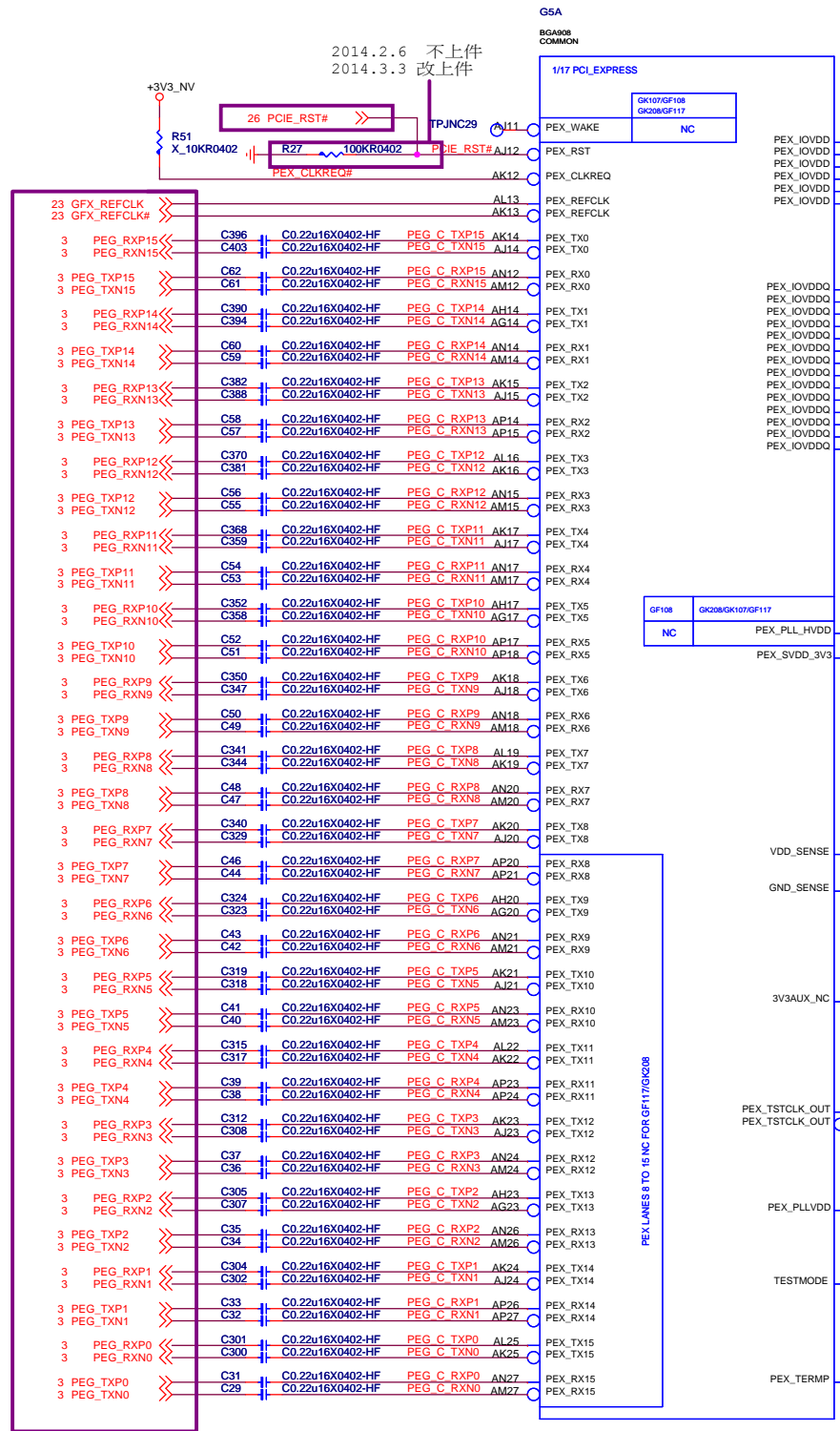
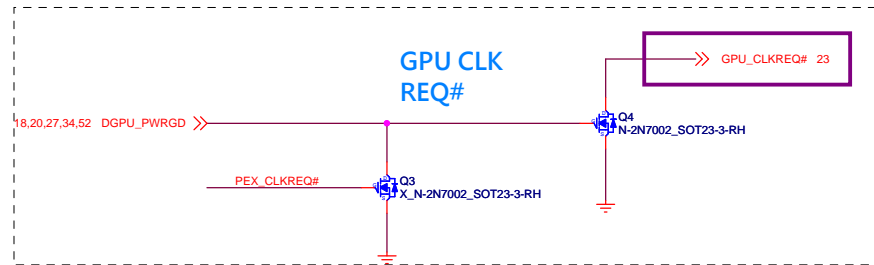
DDR3SODIMM-204PS_BLACK-RH-40
N13-2042000-CK3

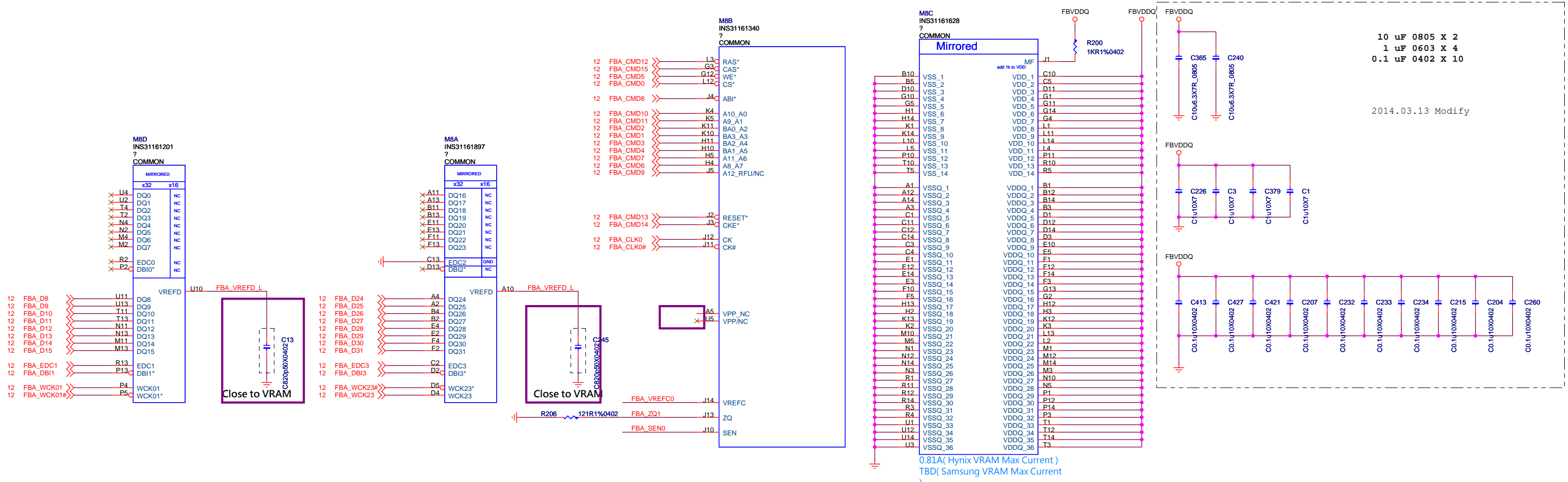
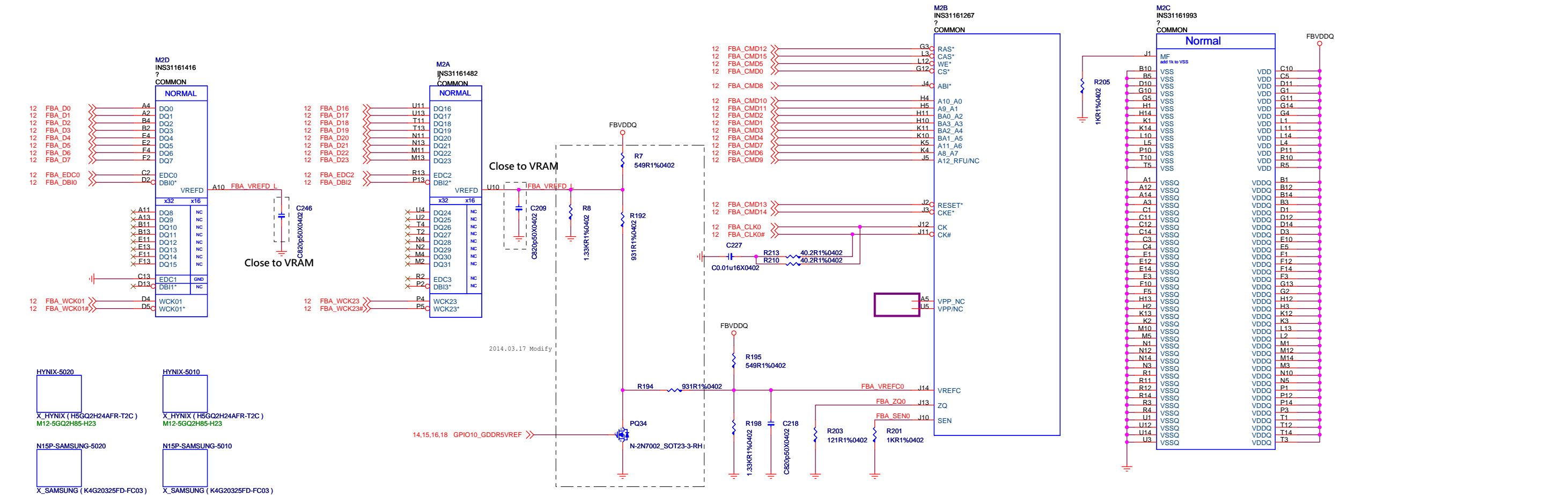
M1(used for S3)
M3(used for S0), maybe to over-ride
Active when soft-start

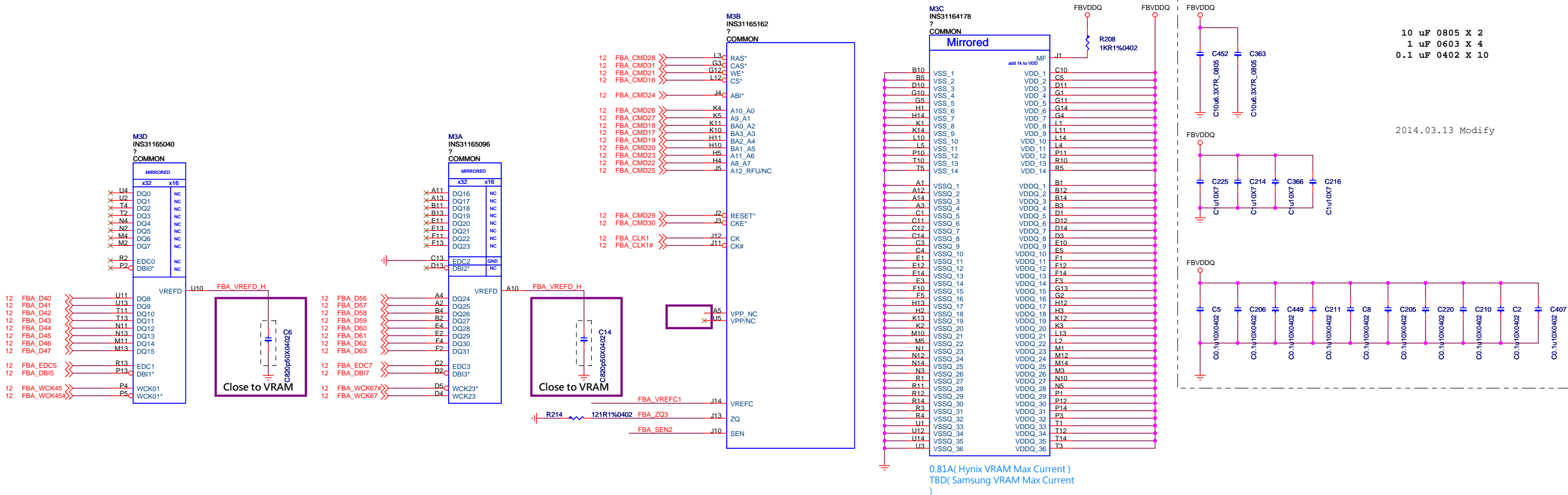
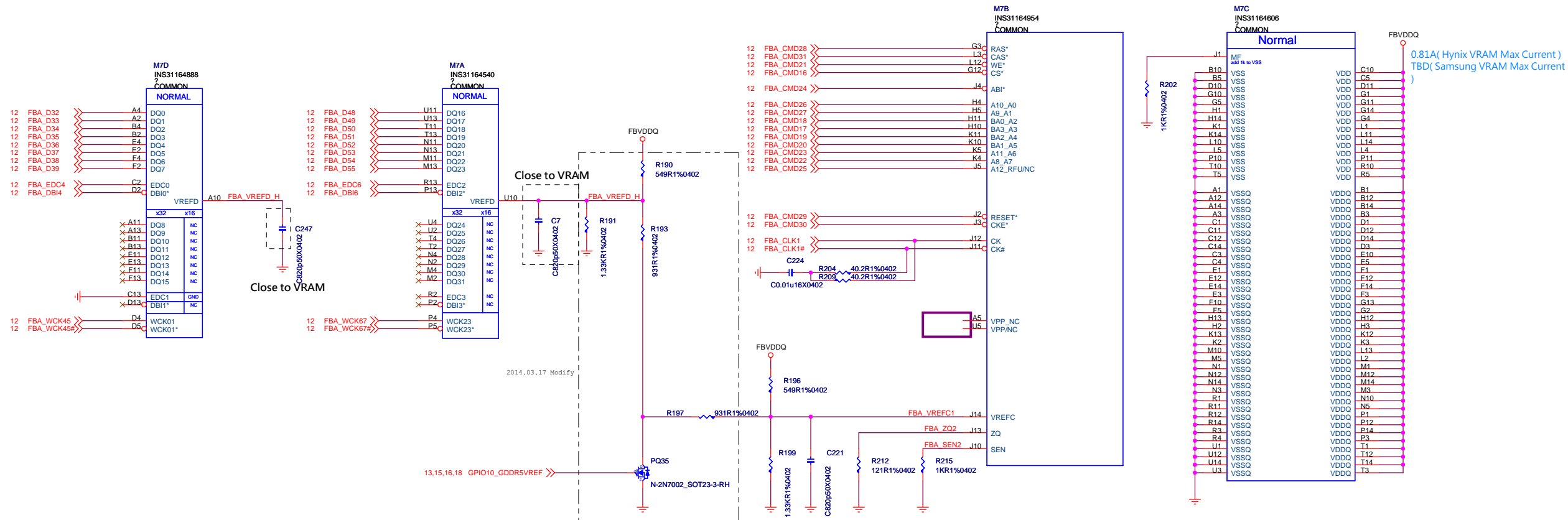


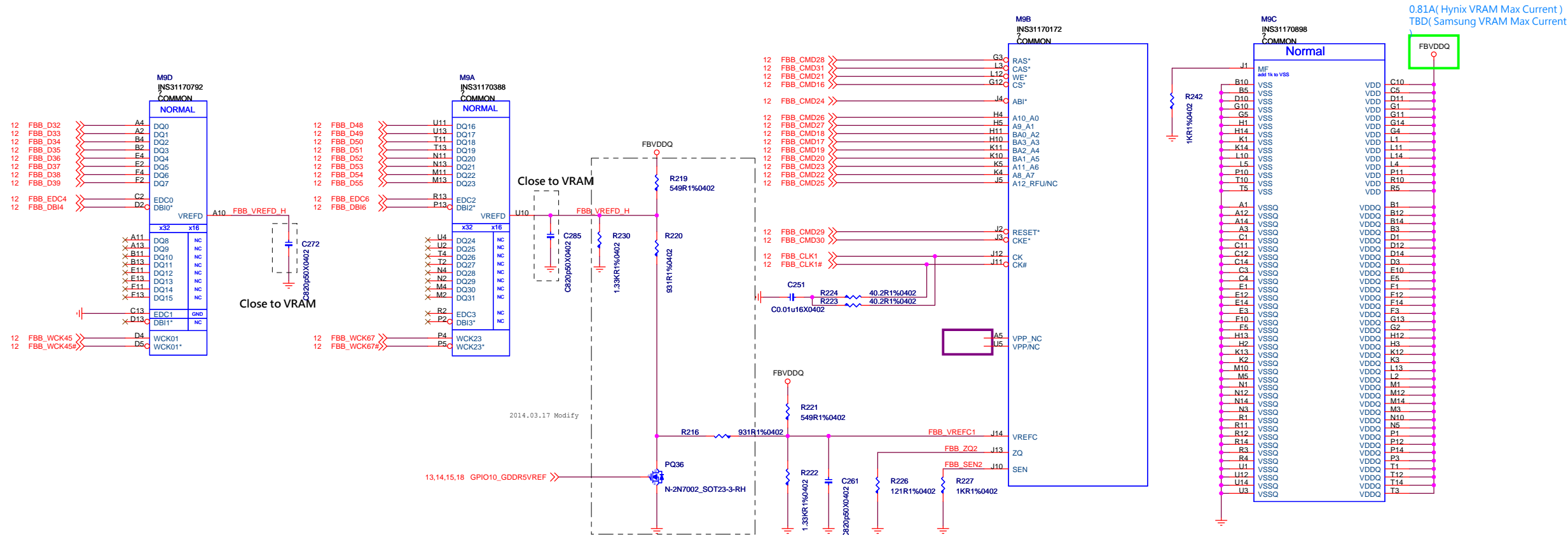
SODIMM#B



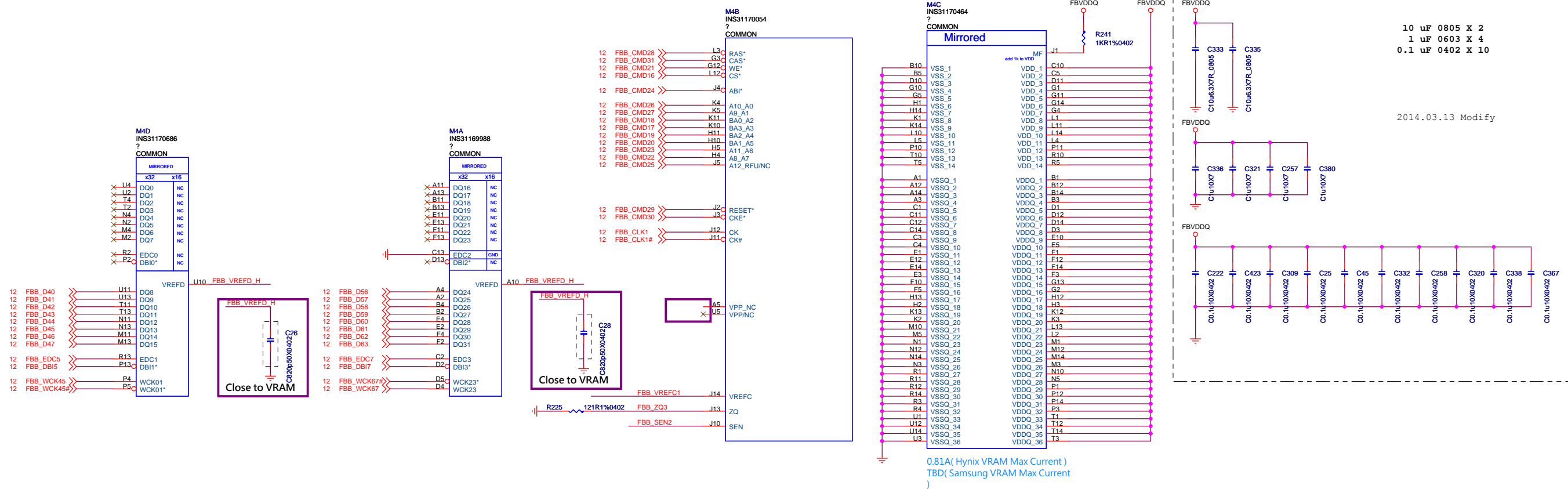






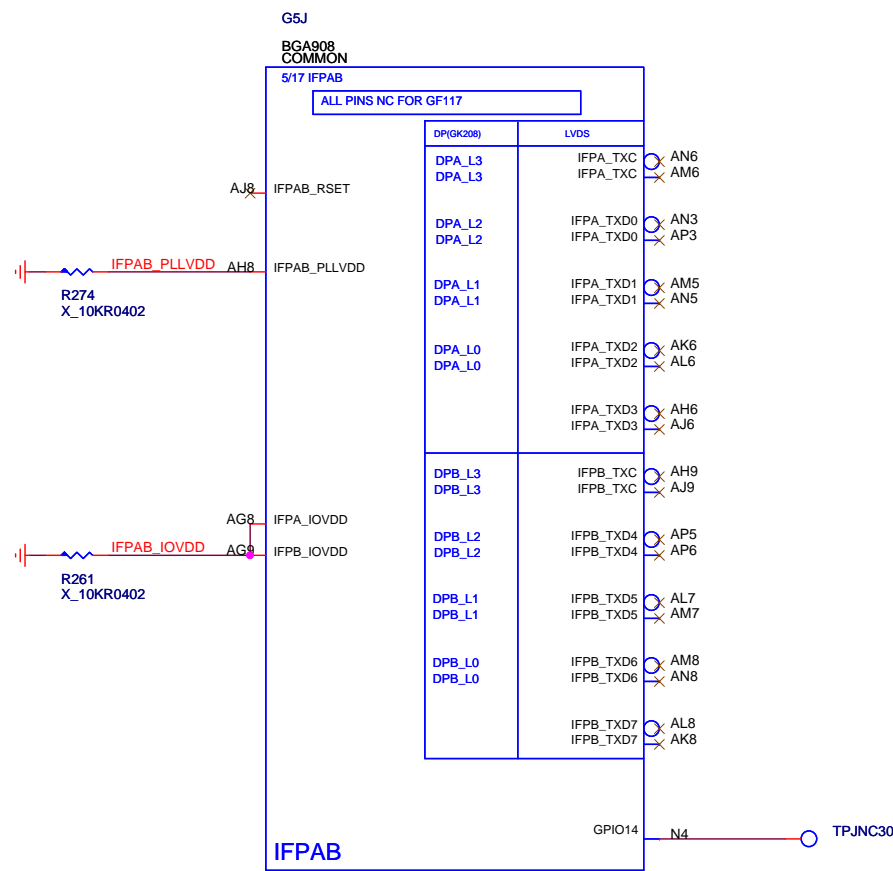


0.81A(Hynix VRAM Max Current)
TBD(Samsung VRAM Max Current)

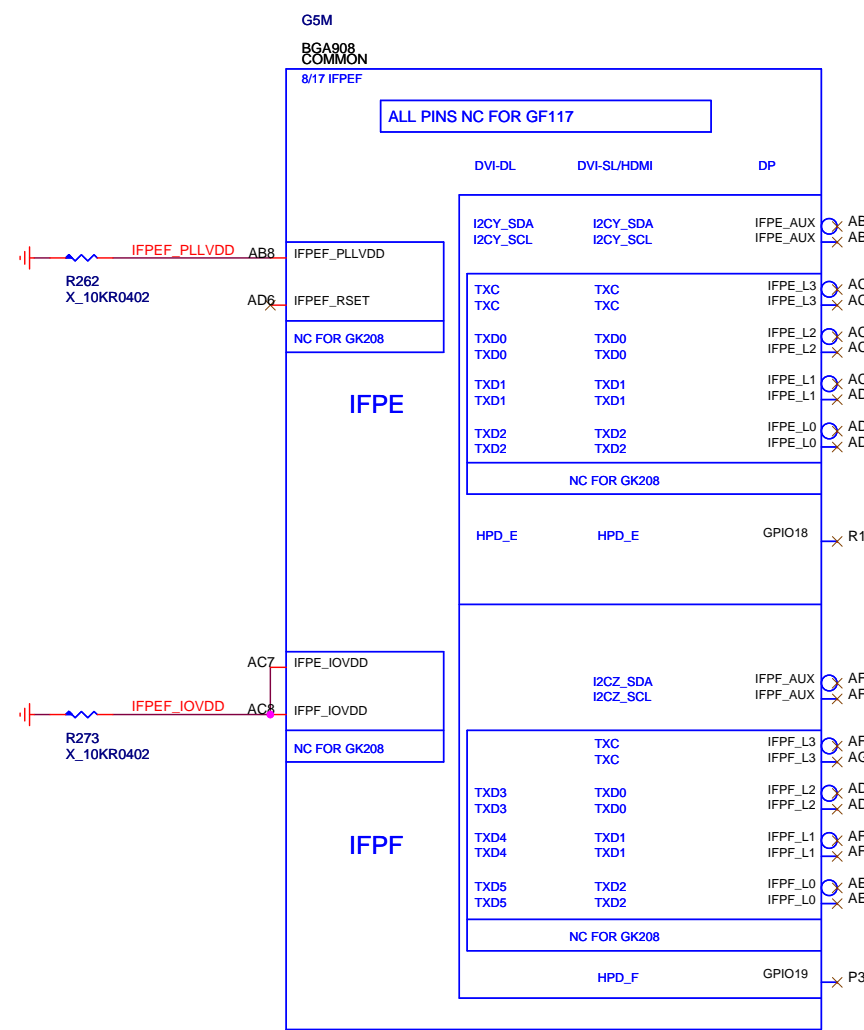


10 uF 0805 X 2
1 uF 0603 X 4
0.1 uF 0402 X 10

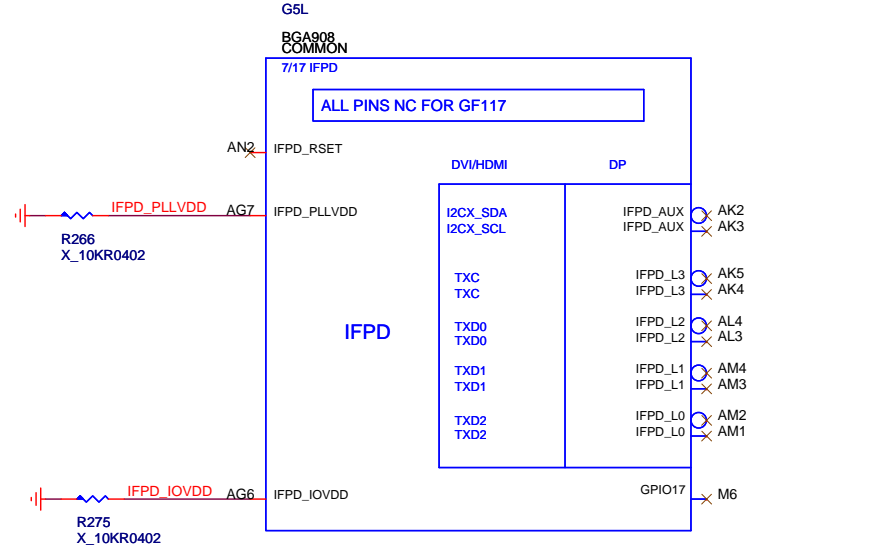
IFP A/B LVDSDual Link



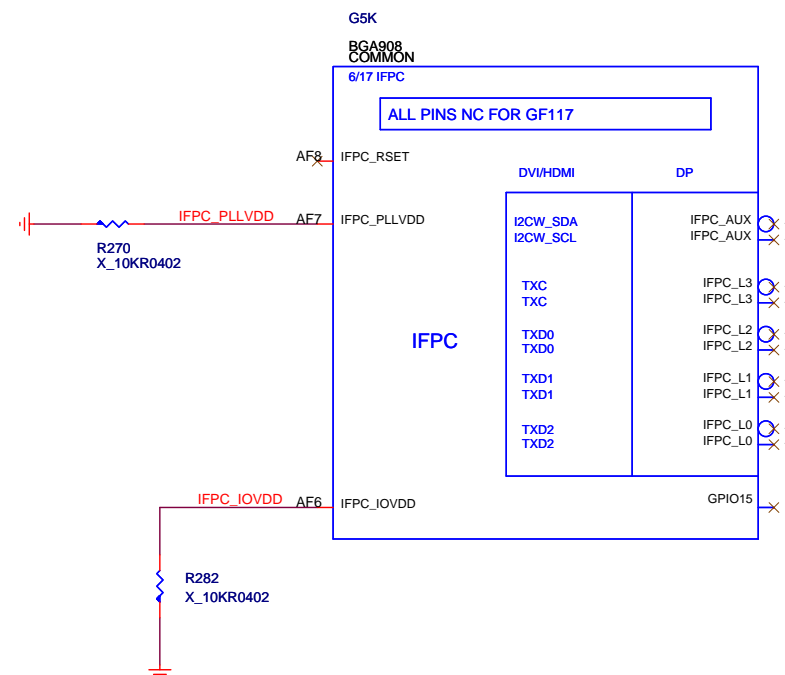
IFP E/F Dual Link TMDS DVI-I



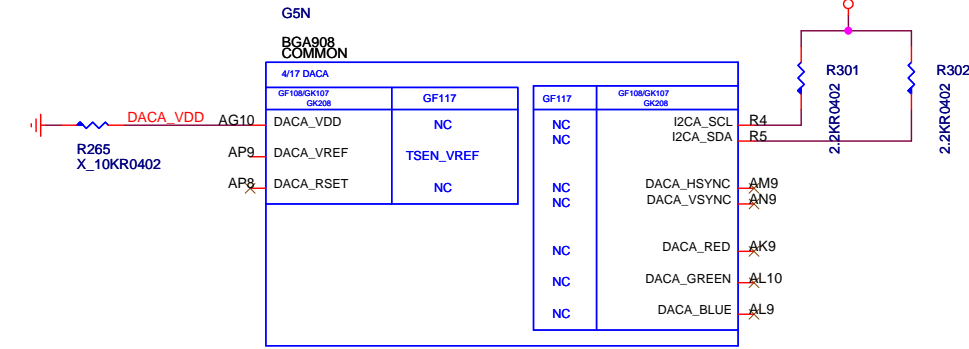
IFP D Dual Mode DP



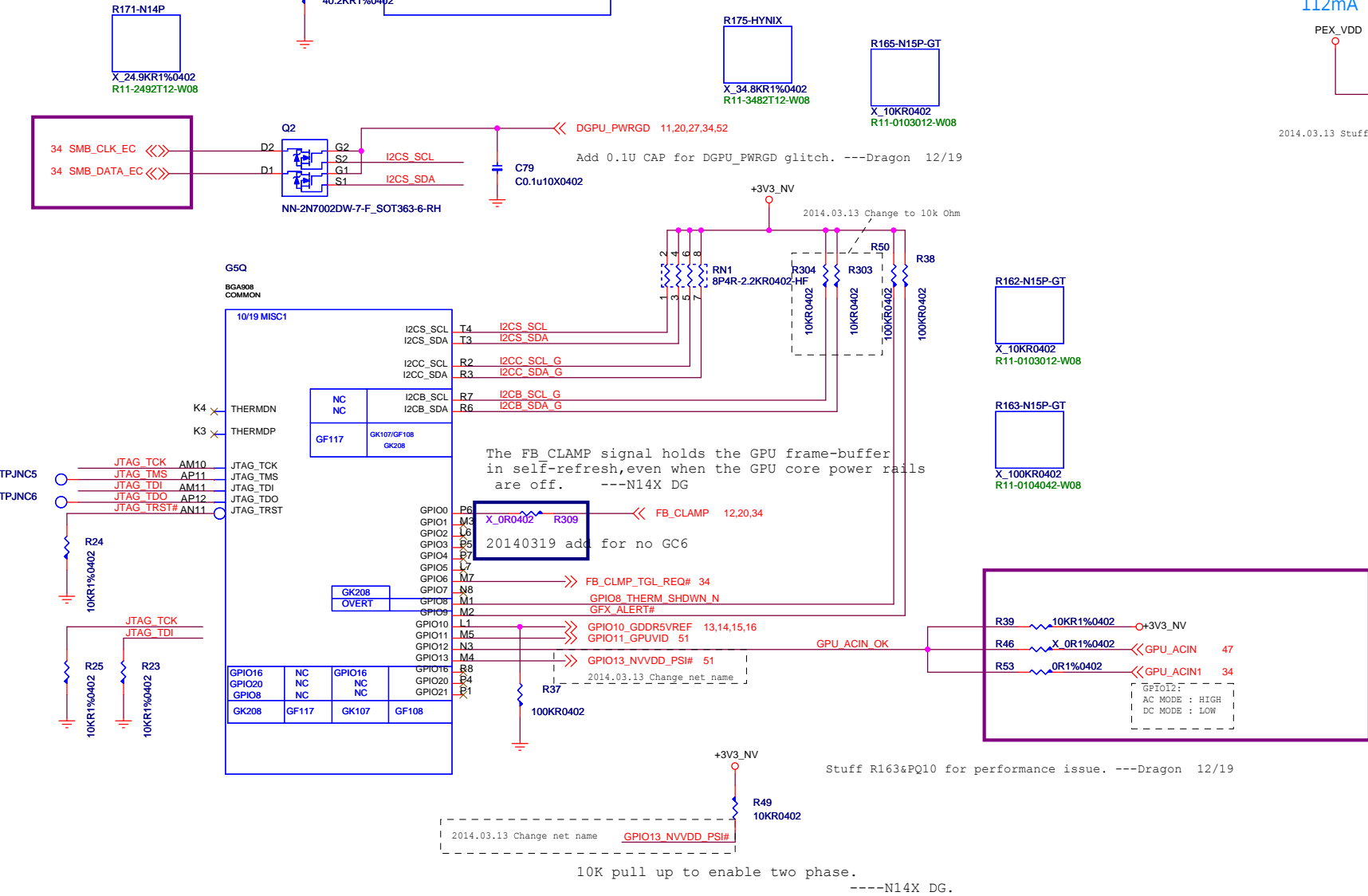
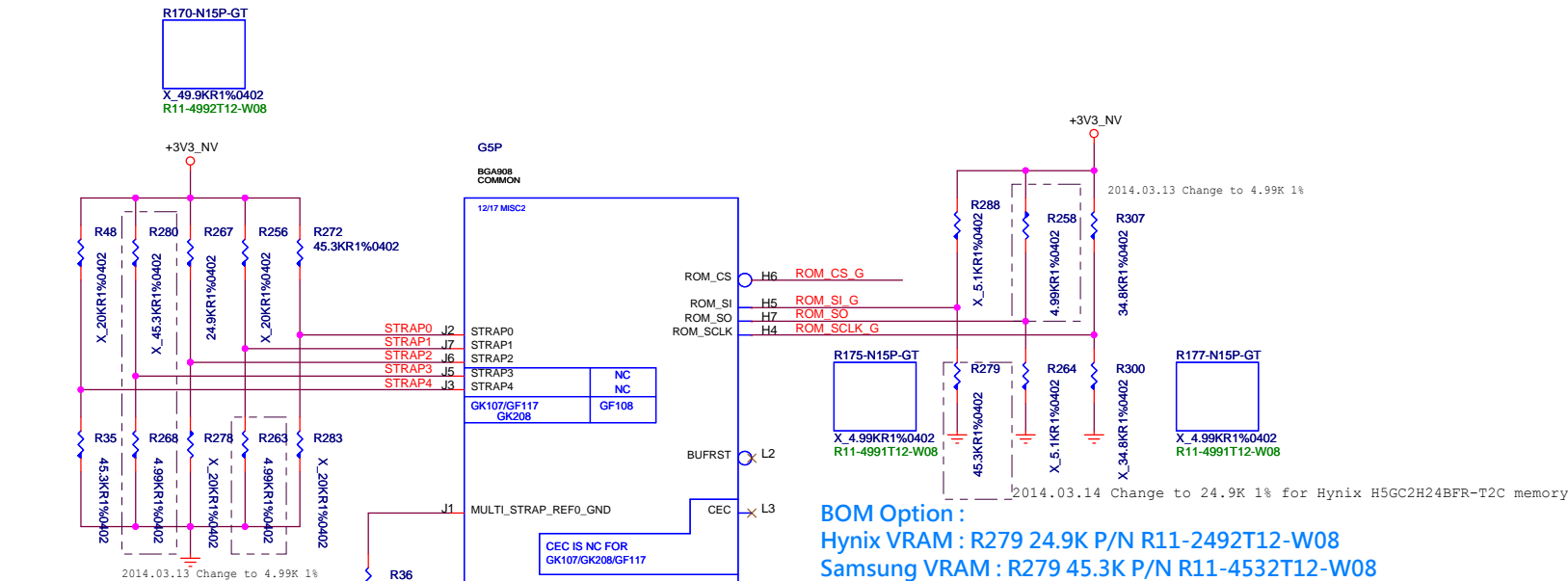
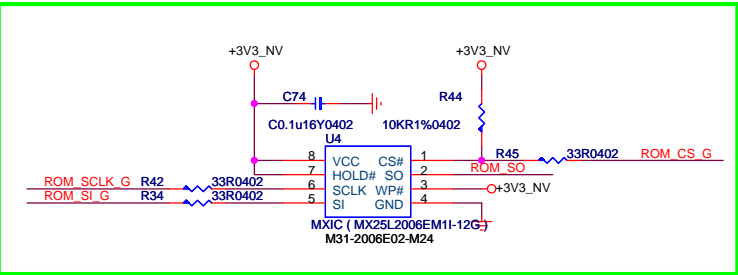
IFP C Native HDMI OR DP



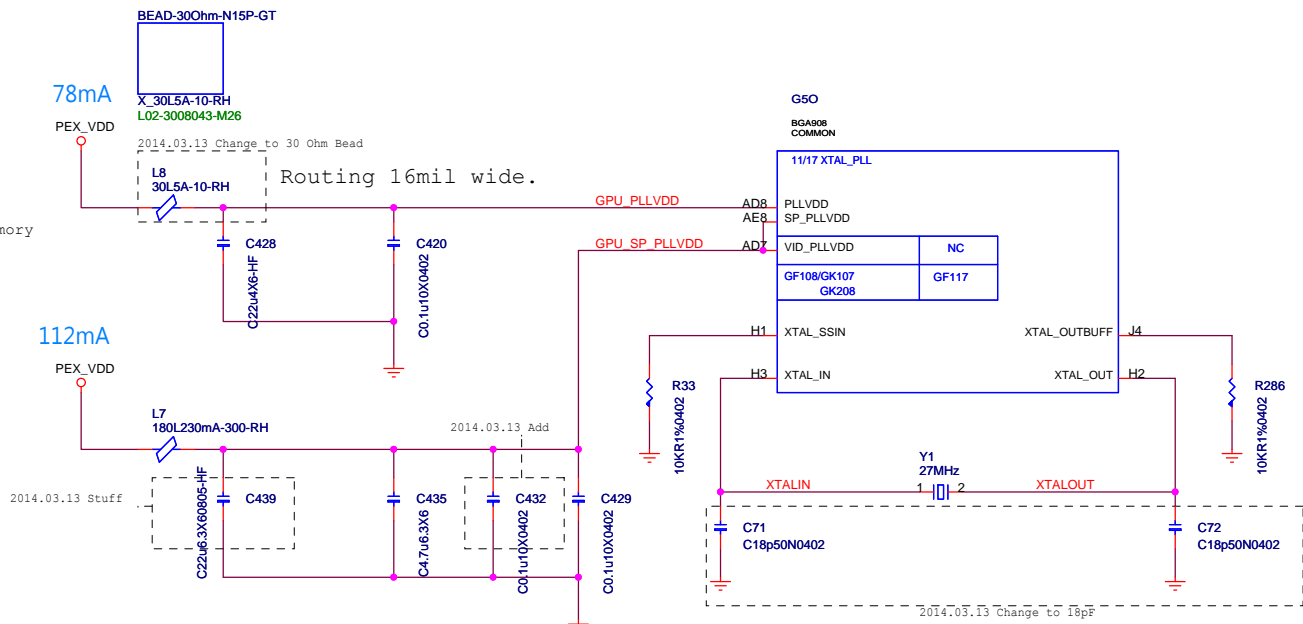
DAC A VGA



external EEPROM

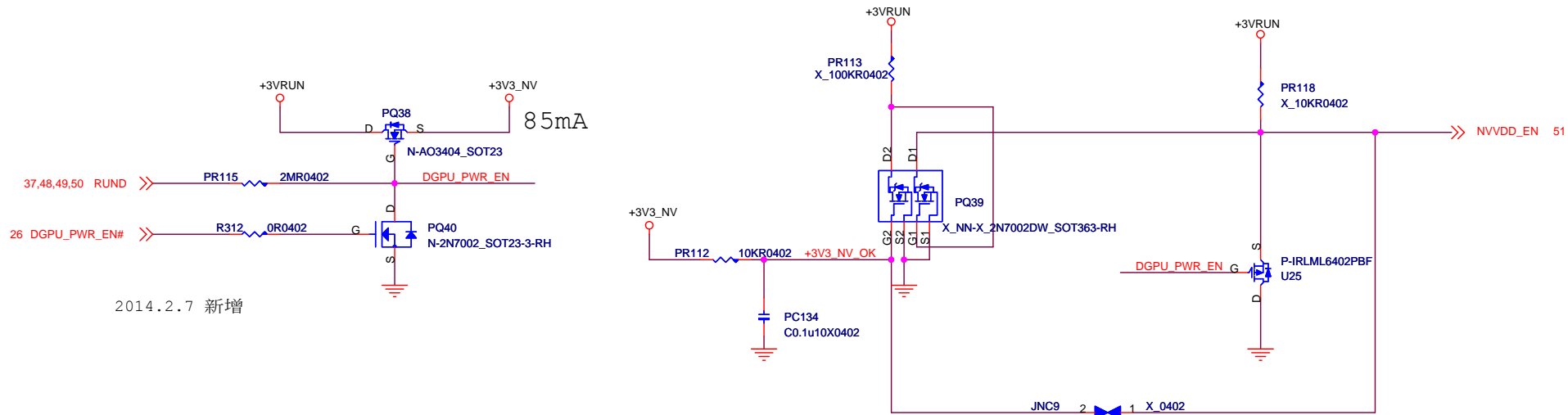


Item	Location	N15P-Q3
Strap Mode	R3365	MULTISTRAP_REF_GND,40.2K PD to GND
Device ID		0x11FC
Package		GB4-128
Memory Type		GDDR5
ROM_SI	R3175	0x4, Hynix 2G, 24.9kohm PD
ROM_SO	R3175	0x7, Samsung 2G, 45kohm PD
ROM_SCLK	R3193	0x8, 5kohm pull up
Strap0	R3170	45kohm pull up
Strap1	R3180	5kohm pull down
Strap2	R3171	DID,0x1100, 24.9kohm PU
Strap3	R3188	0x0 for Optimus, 5kohm pull down
Strap4	R3183	0x0111, 45kohm pull down

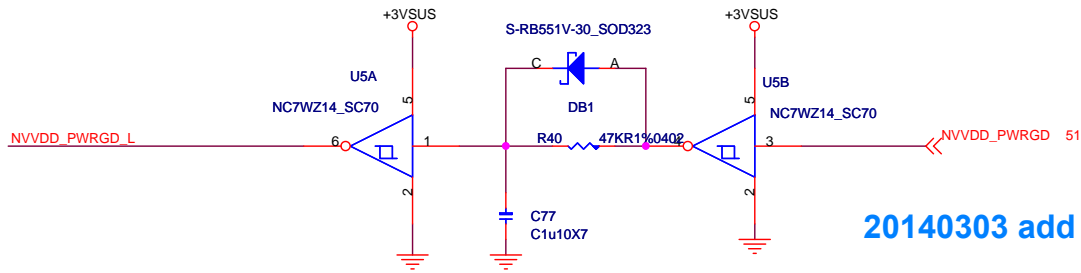
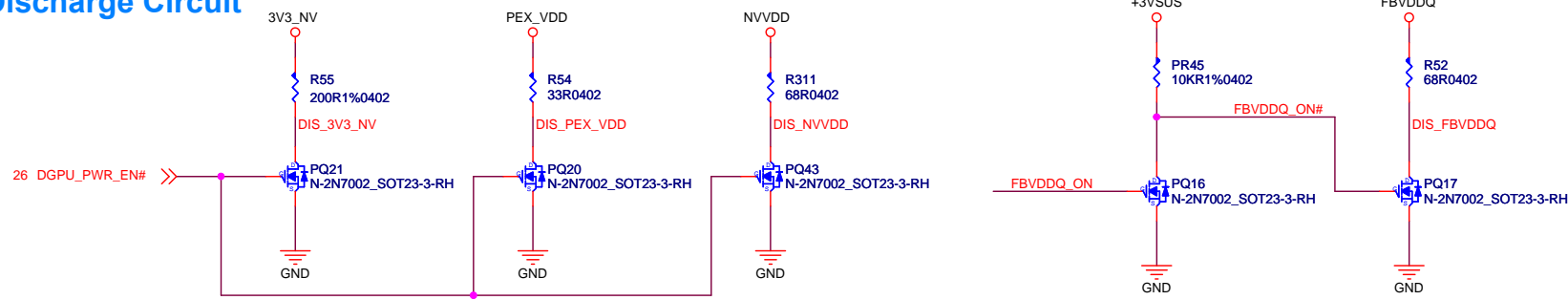


Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	NC	O		
GPIO2	NC	O		
GPIO3	NC	O		
GPIO4	NC	O		
GPIO5	NC	O		
GPIO6	FB_CLAMP_TGL_REQ	O	FB Clamp toggle request	
GPIO7	NC	O		
GPIO8	OVERT	I	Thermal Over Temperature	100K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect	100K pull-up
GPIO13	SPI	O	Phase Shedding	10K pull-up
GPIO14	NC	I		
GPIO15	NC	I		
GPIO16	NC	O		
GPIO17	NC	I		
GPIO18	NC	I		
GPIO19	NC	I		
NC	NC			

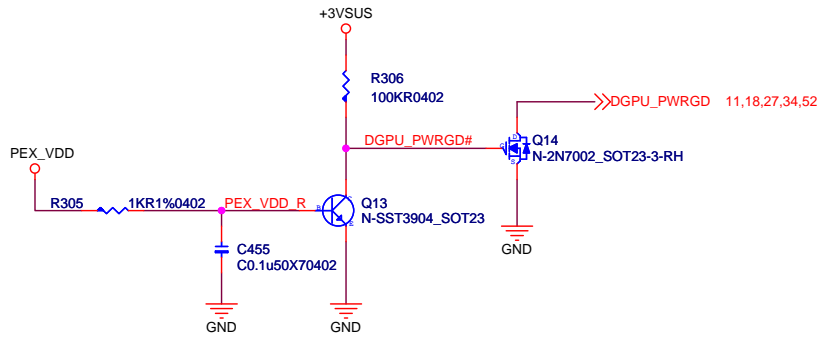
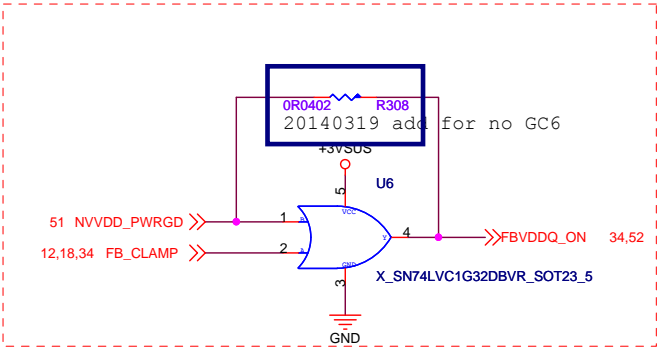
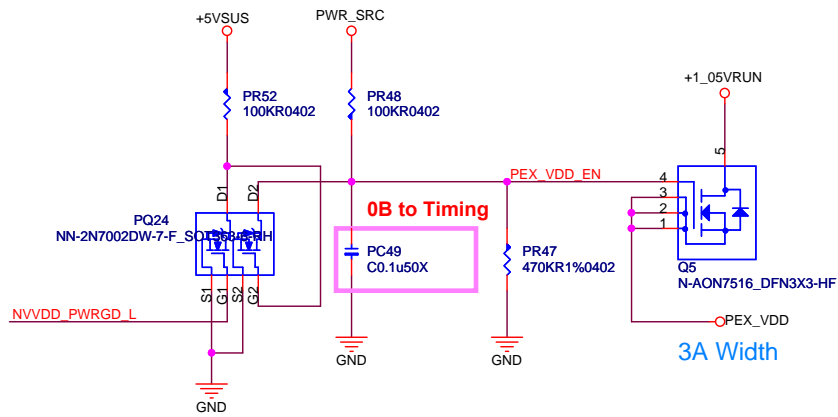
DGPU_Power Control



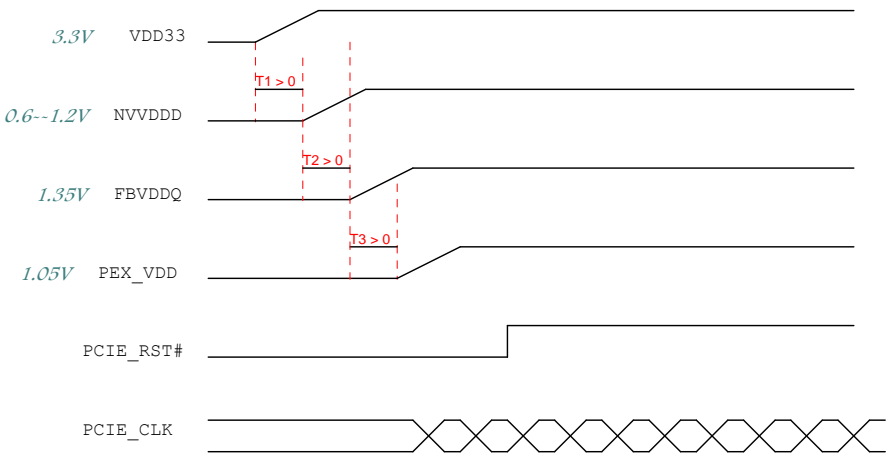
Discharge Circuit



PEX_VDD



GPU POWER ON SEQUENCE



NOTES: The ramp time for any rail must be more than 40 us.
The total time for all rails to ramp up should be within 6ms.
A power rail has to ramp up to 90% before the next rail in sequence can start ramping up.
No signal should be applied to the GPU before the power rails are fully ramped

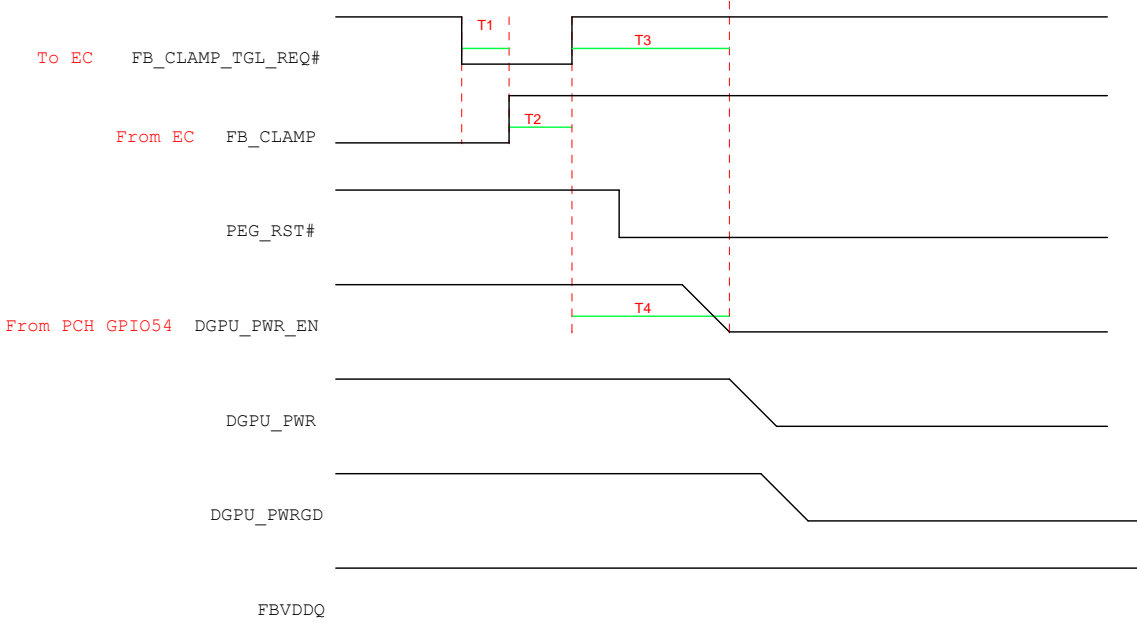
NOTES: For optimus system, VDD33 usually drops down earlier than NVVDD and FBVDDQ.
NOTES: All rails must be powered off within 10 ms from the first rail powering off.

GC6 TIMING

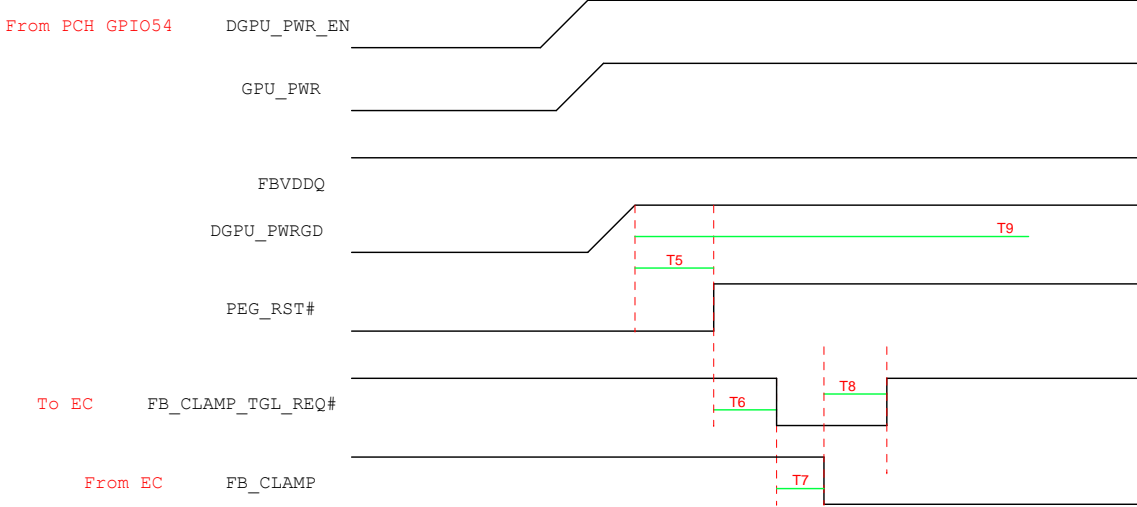
	Min	Max	Unit	Description
T1	0	10	mS	GPU asserts toggle request to GB_CLAMP assertion
T2	0	1	mS	Assertion of FB_CLAMP to de-assertion of toggle request
T3	0	10	mS	De-assertion of toggle request to GPU_PWR_EN=0
T4	0.01	1	mS	PEX reset assertion to GPU_PWR_EN de-assertion
T5	0.1	5	mS	GPU power stable to de-assertion of PEX reset
T6	3.3		mS	De-assertion of PEX reset to toggle request assertion
T7	0	1	mS	Assertion of toggle request to de-assertion of FB_CLAMP
T8	0	1	mS	De-assertion of FB_CLAMP to de-assertion of toggle request
T9	TBD	TBD	mS	GPU power enable to GPU ready for normal operation

Notes: *System designers should minimize T1,T3,T4,T5,T6,and T7 to increase the time spent in GC6.
This increased GC6 residency will improve both power savings and user experience.
**If10 ms expires for T1, the GPU will de-assert FB_CLAMP_TGL_REQ# and abort the GC6 entry procedure.
FB_CLAMP should never assert outside an FB_CLAMP_TGL_REQ# handshake.

GC6 ENTRY SEQUENCE (NOT support)

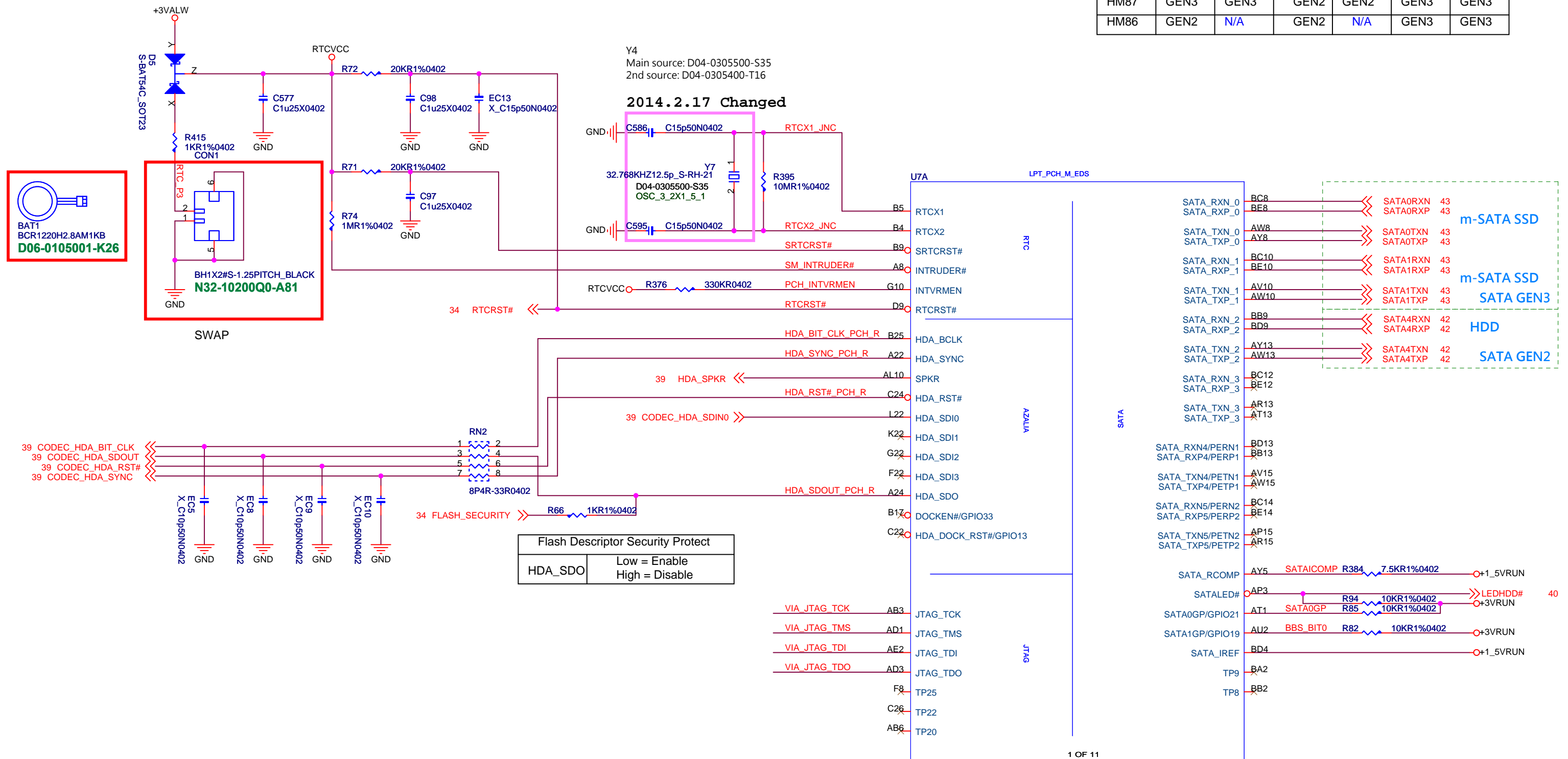


GC6 EXIT SEQUENCE



Lynx Point (HDA/JTAG/SATA)

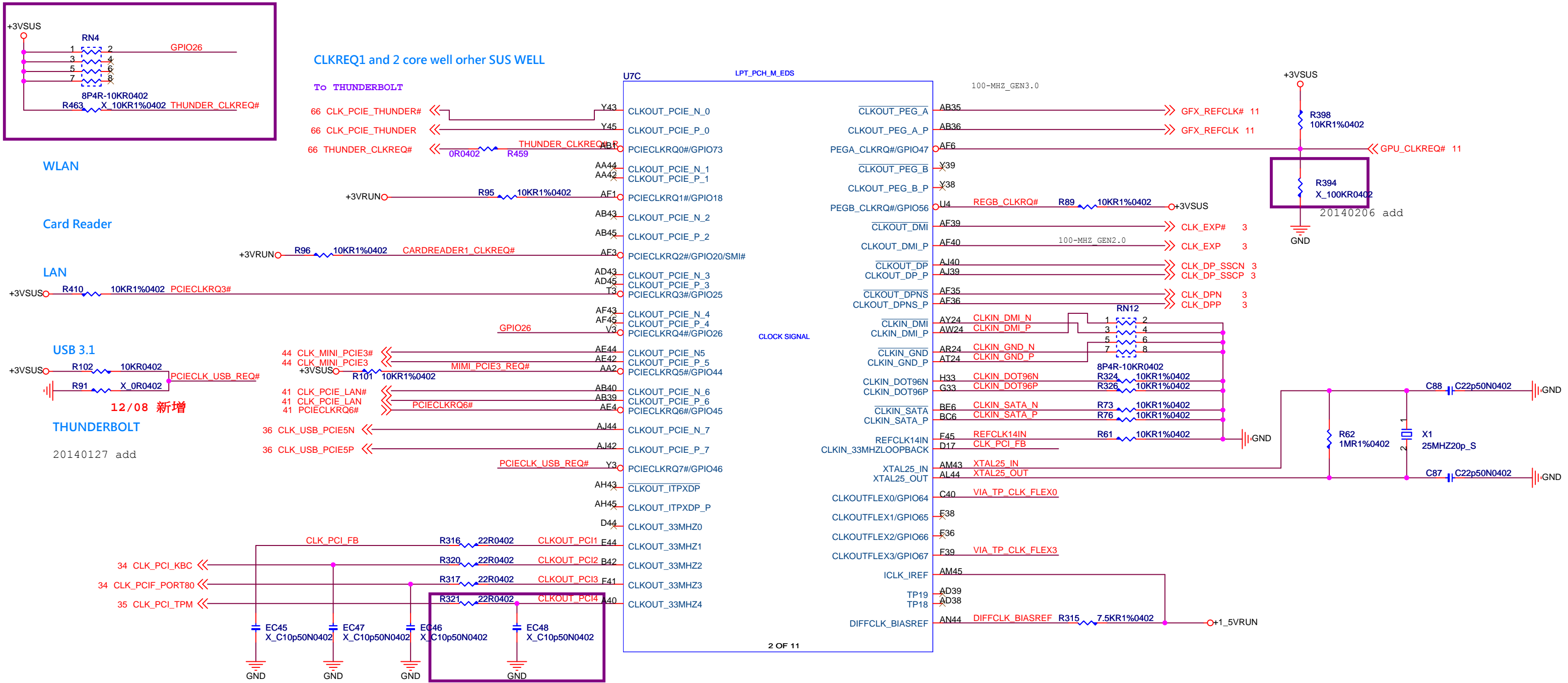
SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



SPK	<p>The Signal has a weak internal pull-down</p> <p>Note: the internal pull-down is disabled after PLTRST# deasserts.</p> <p>If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)</p>
-----	--

Lynx Point (Clock)

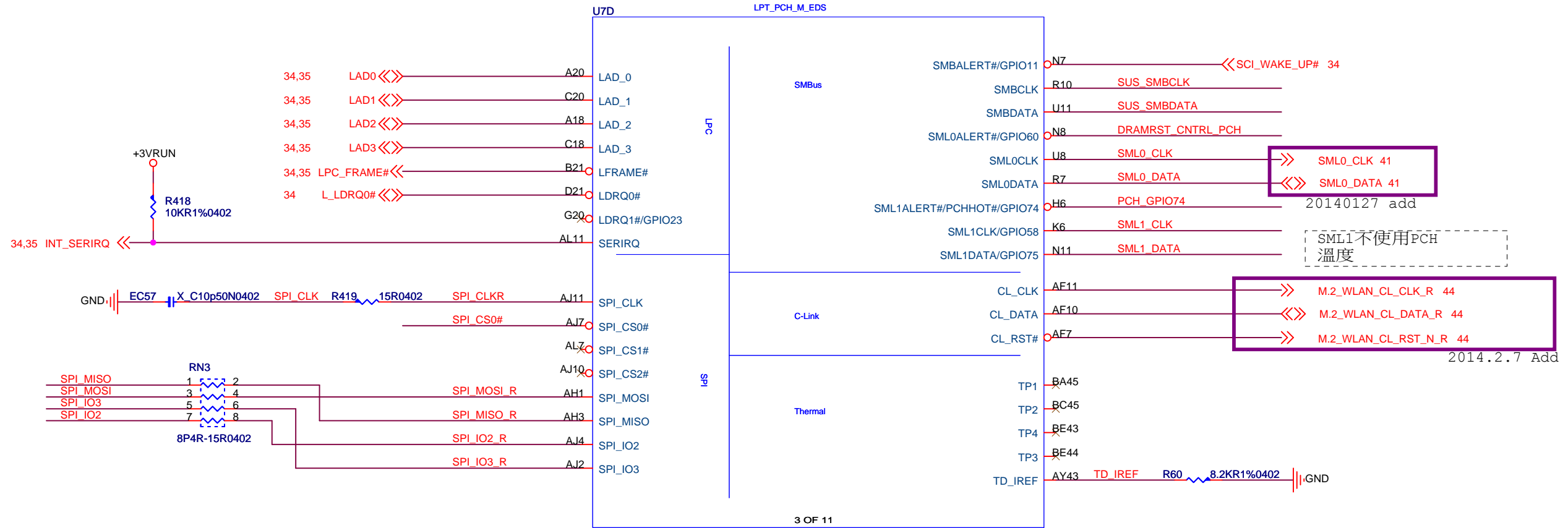
PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



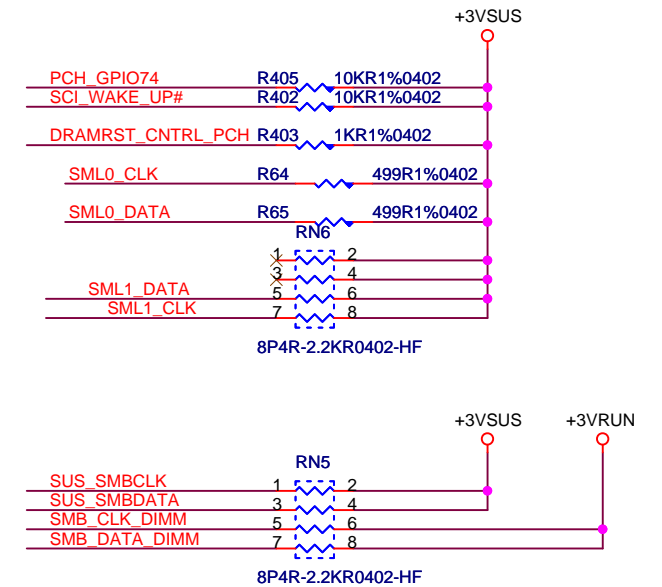
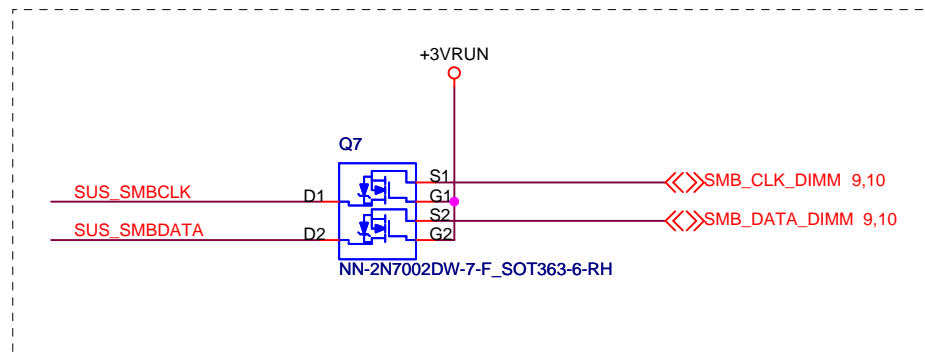
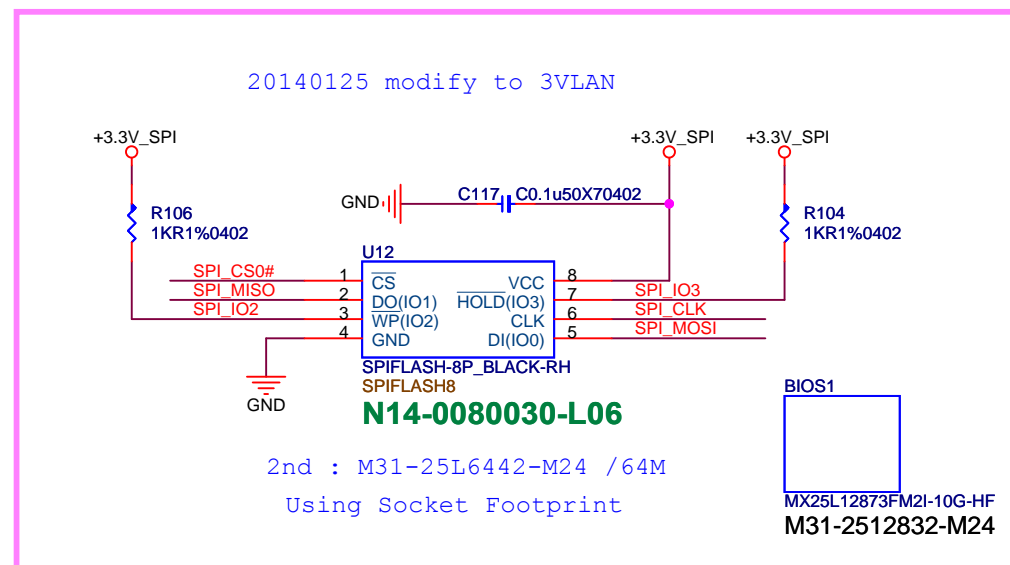
2014.2.17 Add

The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

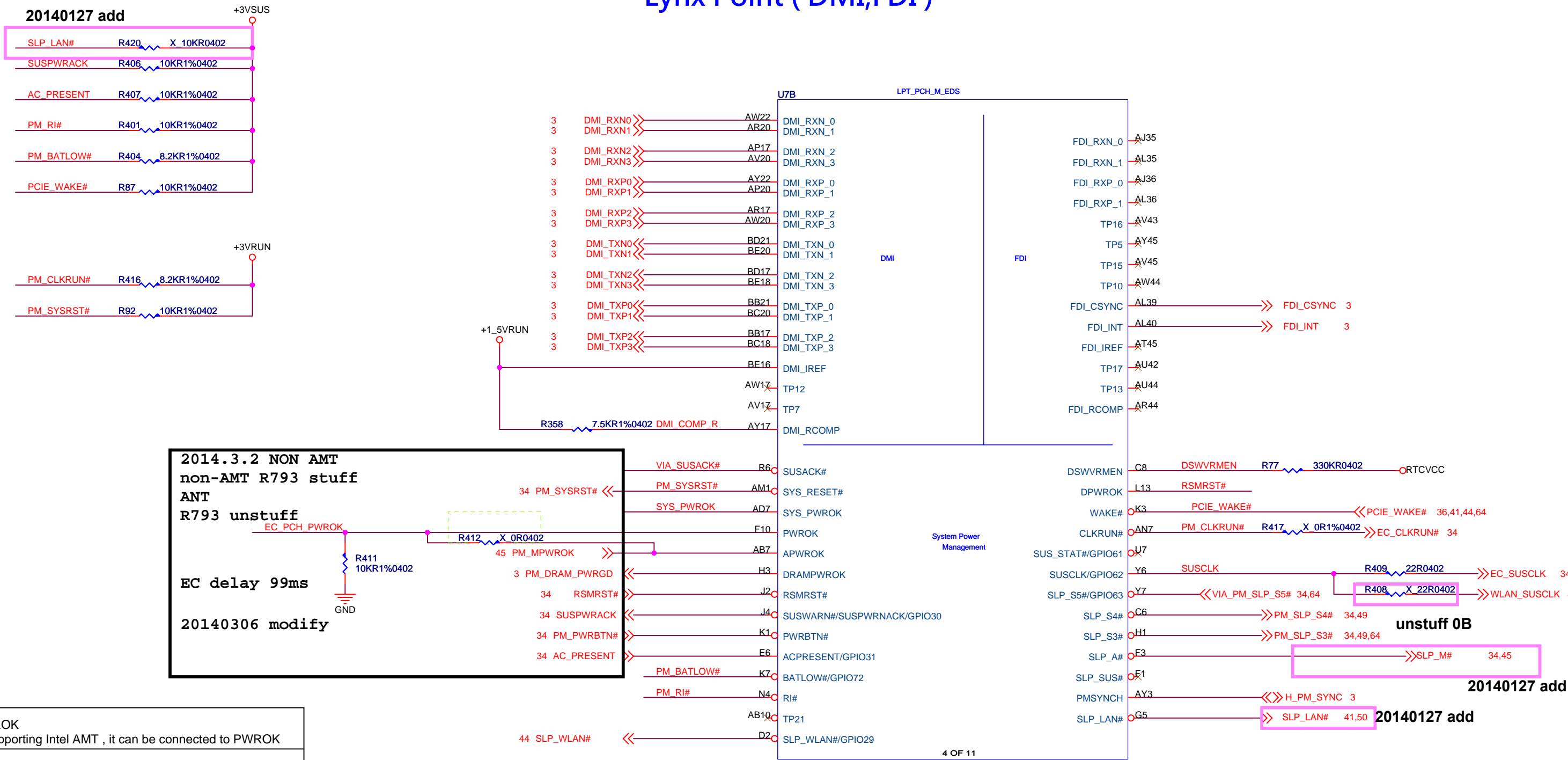
Lynx Point (LPC,SMBUS)



20140310 0A先上socket,N14-0080030-L06
顆粒,M31-25Q6402-E17
(0A Footprint共用SPIFLASH8 is Socket footprint)



Lynx Point (DMI,FDI)

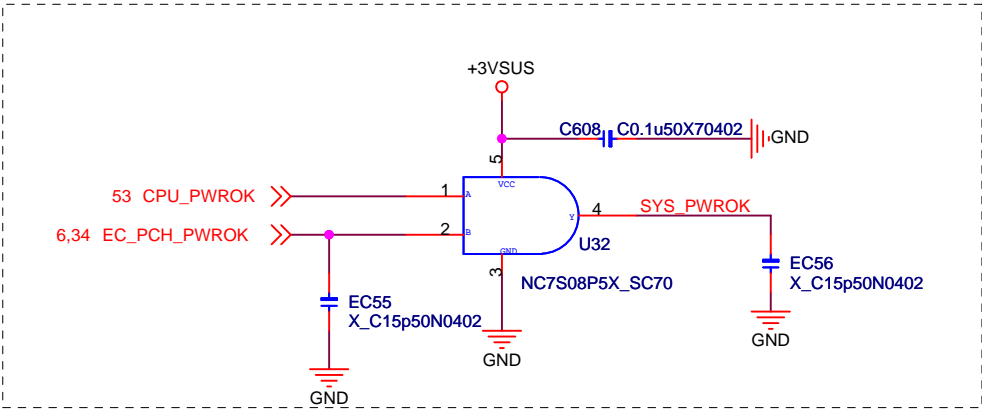


APWROK
not supporting Intel AMT , it can be connected to PWROK

GPIO31 : If not used,require pull up +3VSUS

DSWVRMEN - On Die DSW VR Enable
HIGH : Enable internal 1.05V regulator
LOW : Disable

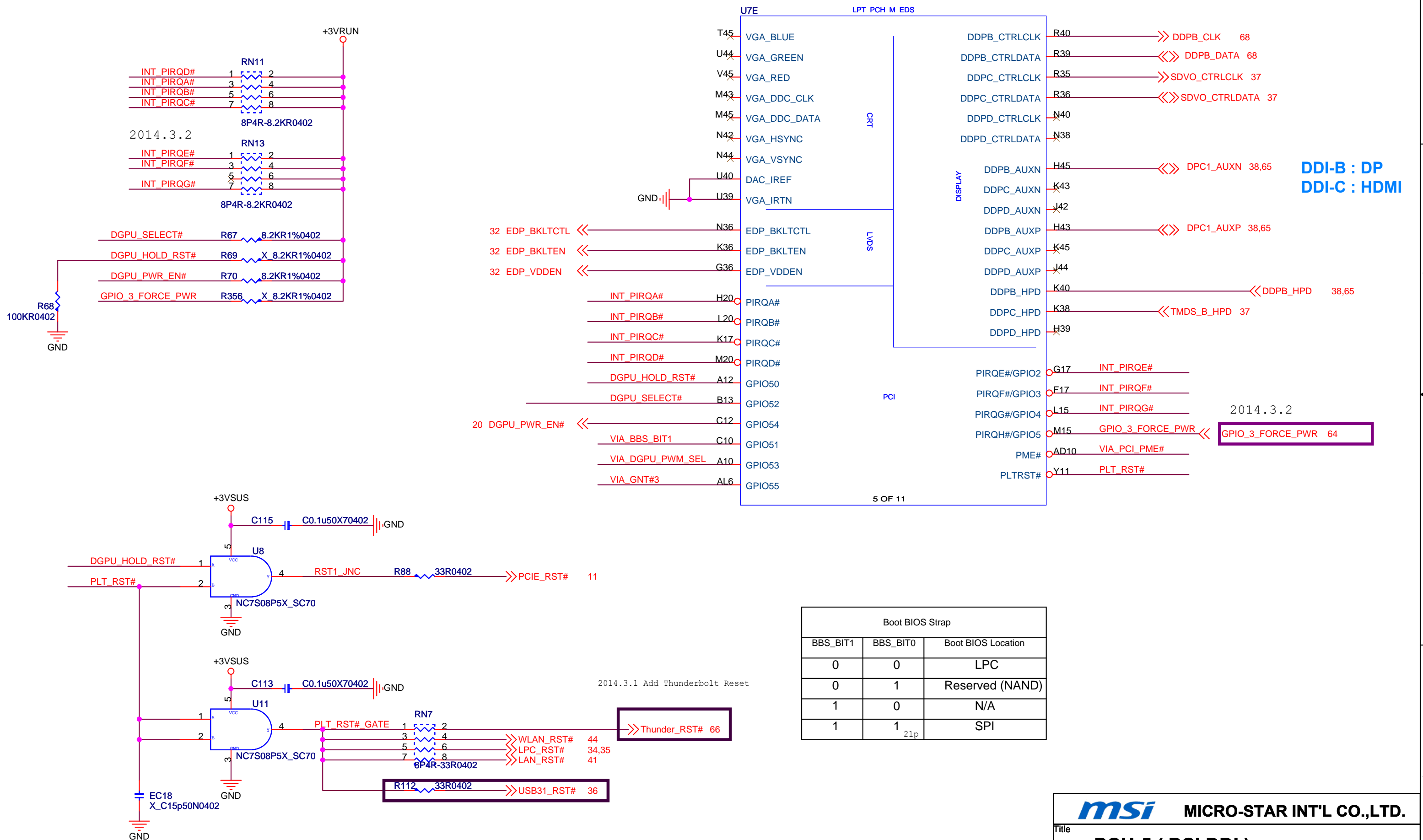
DPWROK
Without deep s4/s5 support tied together with RSMRST#



GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

Lynx Point (PCI,DDI)



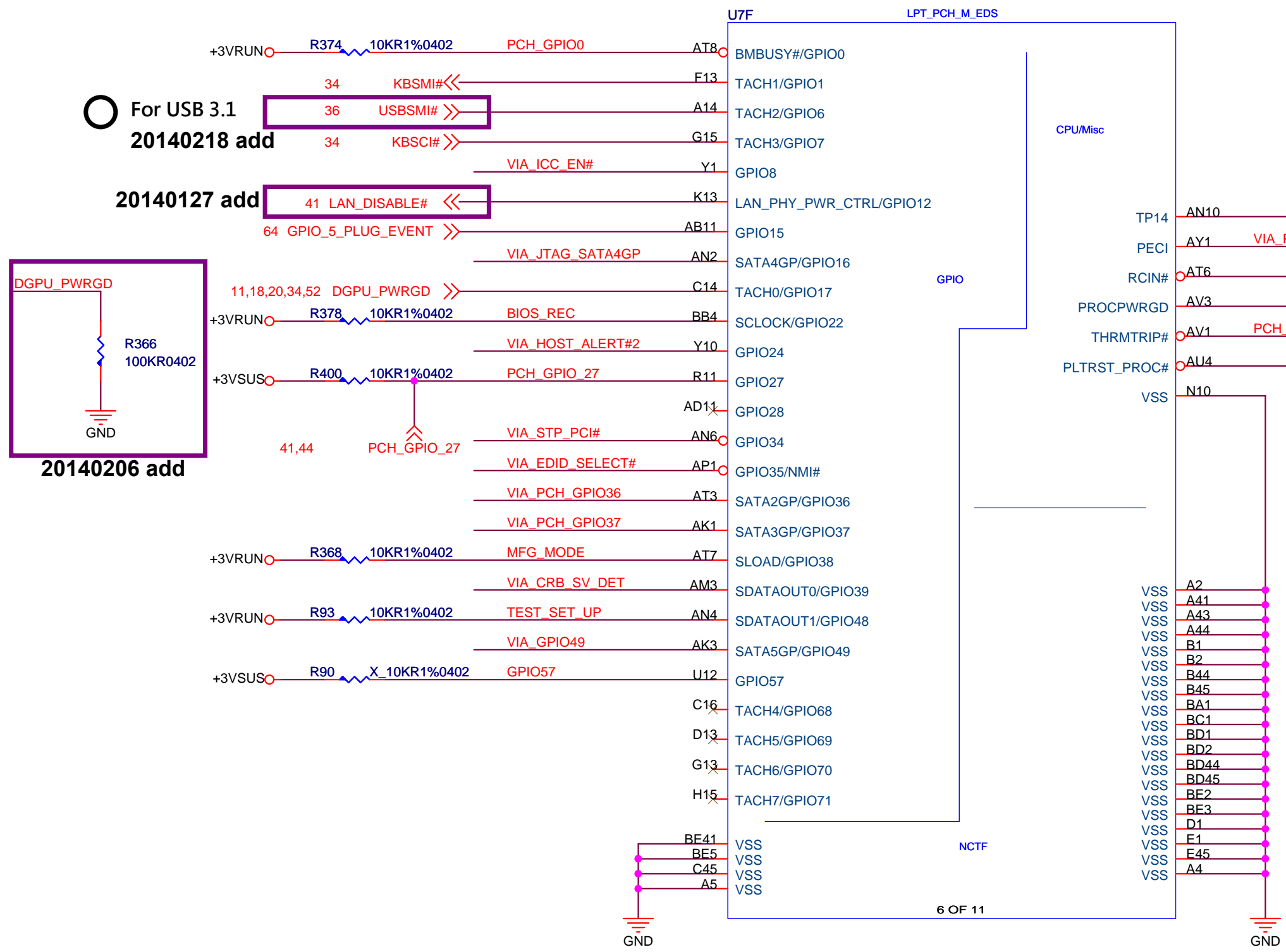
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

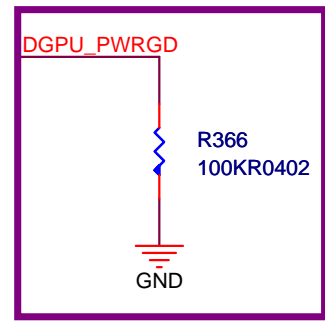
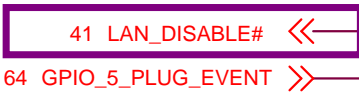
公板100R
empty



For USB 3.1
20140218 add

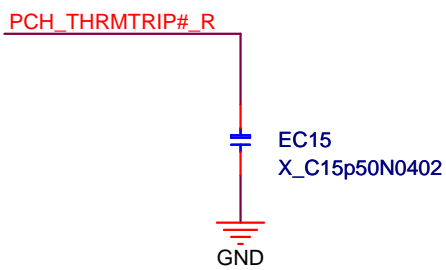
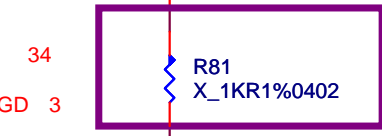


20140127 add



20140206 add

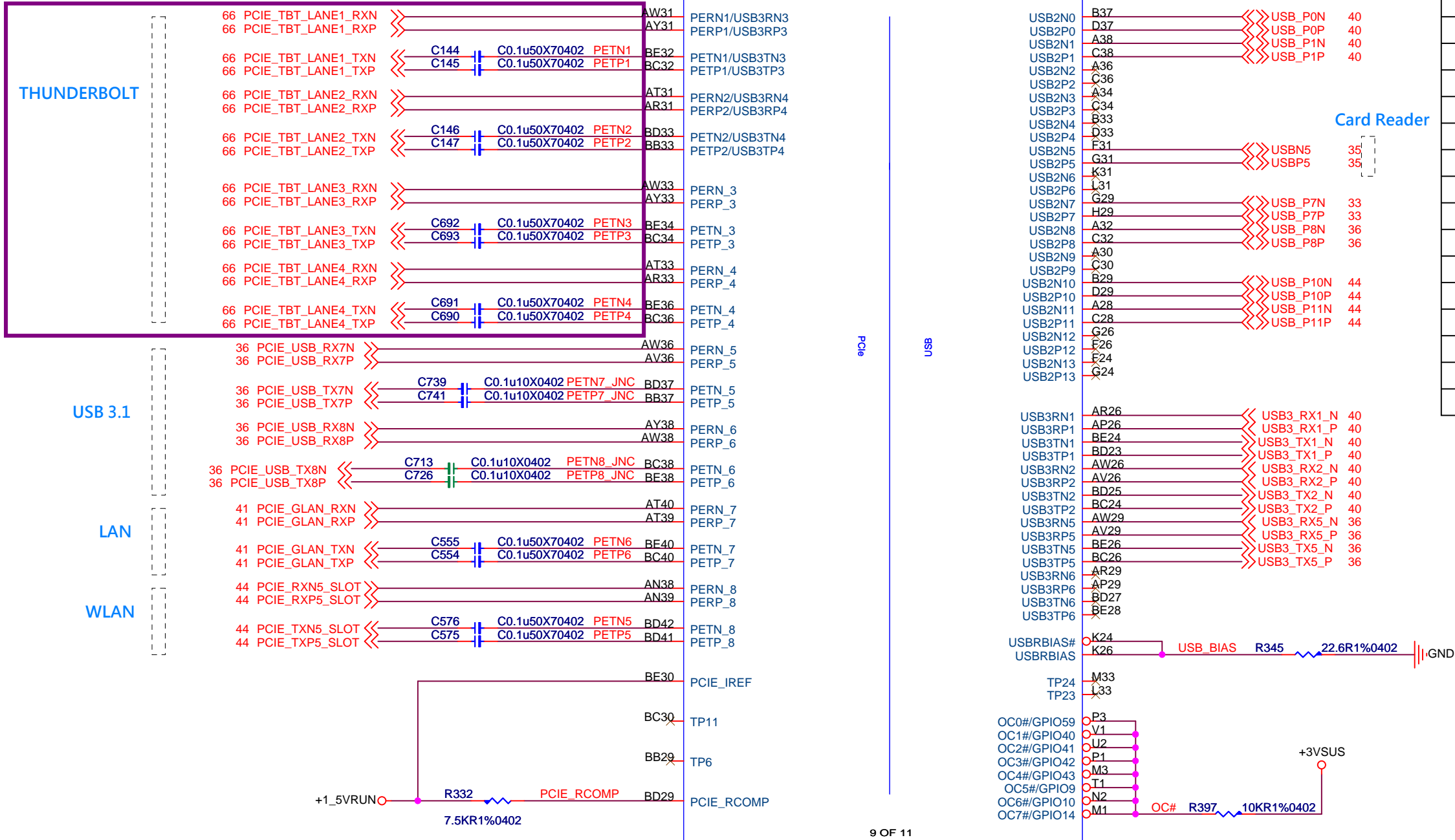
	Haswell	Boardwell
R81	No Stuff	Stuff
R80	Stuff 390R	Stuff value need to confirm



Lynx Point (PCIE,USB)

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9

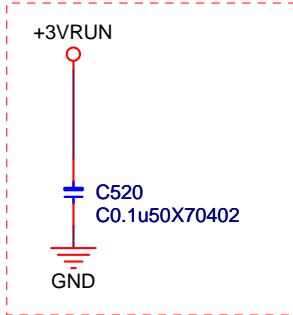
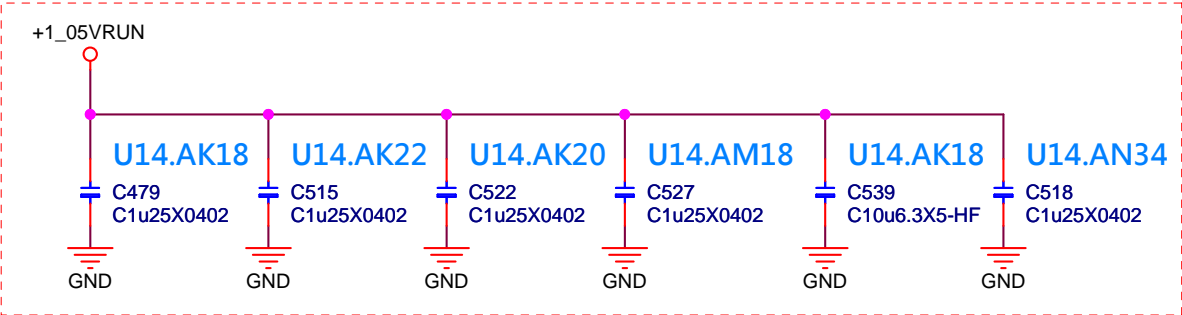
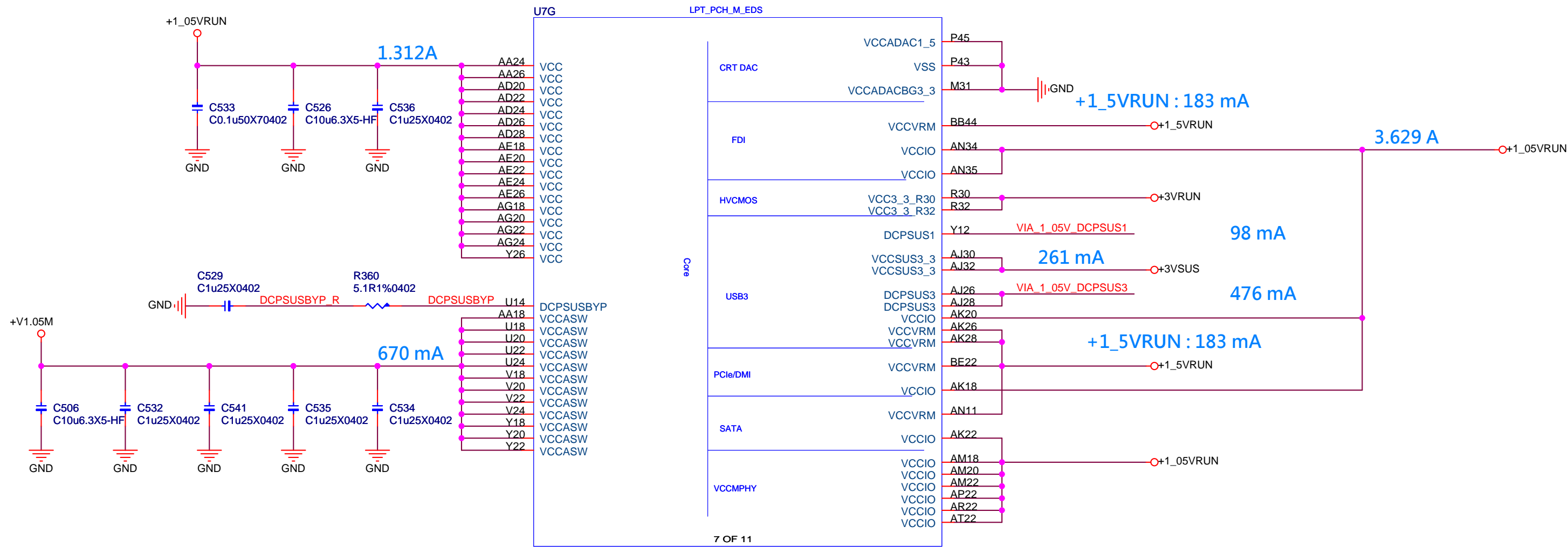
2014.2.24 Modify to four lanes TBT



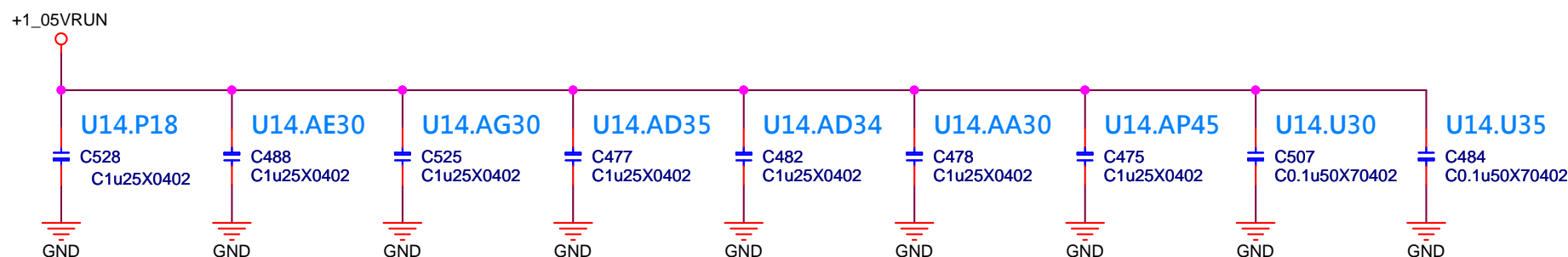
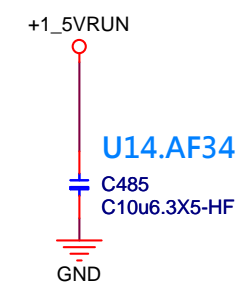
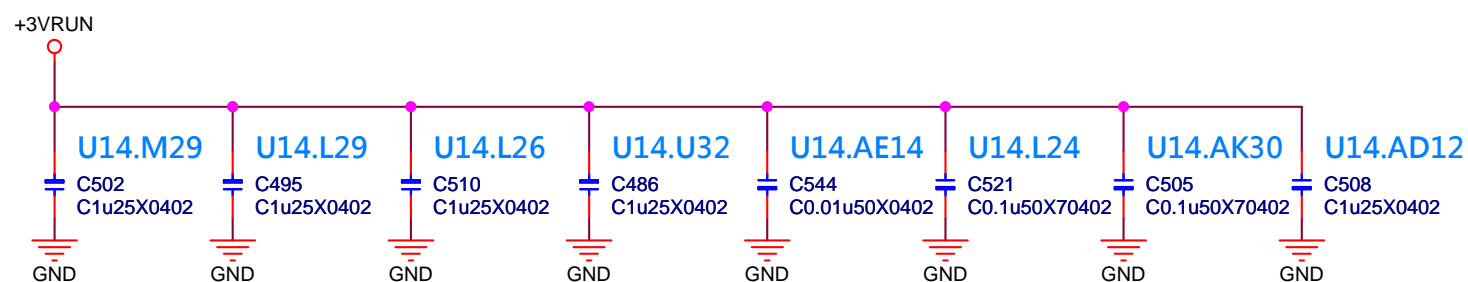
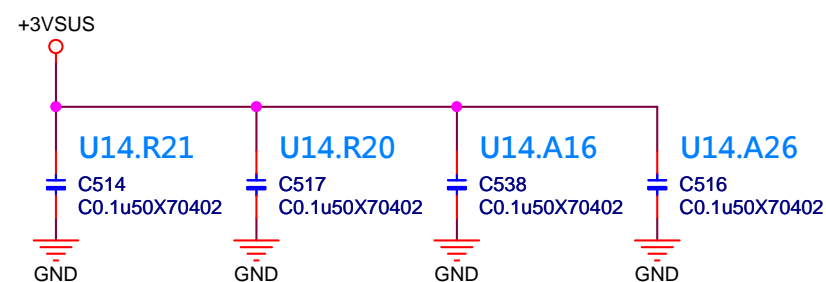
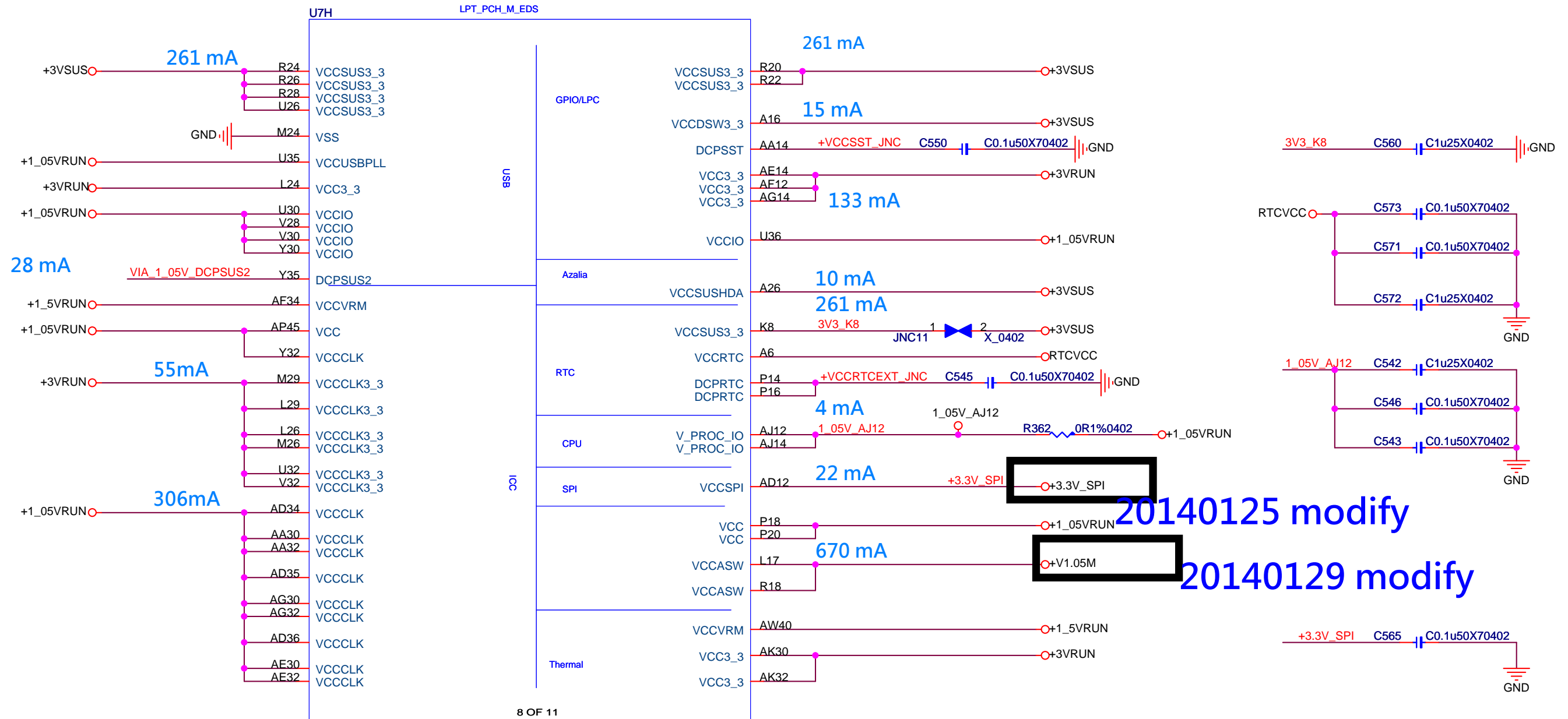
USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16H3A
1	2	USB 3.0 Port 2	16H3A
2			
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	16H31
9	4	USB 3.0 Port 6	no use
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

HM86 沒USB3.0 PORT 5,6

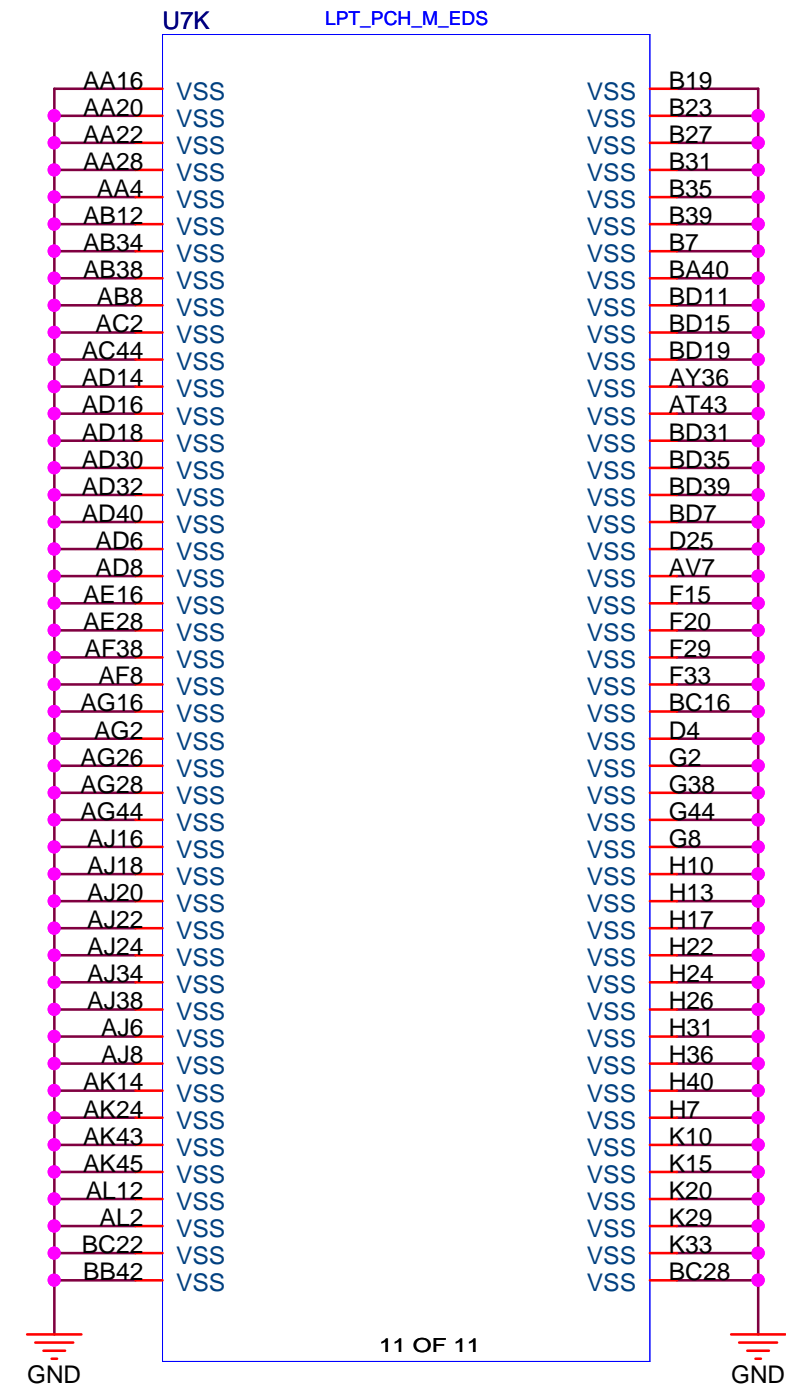
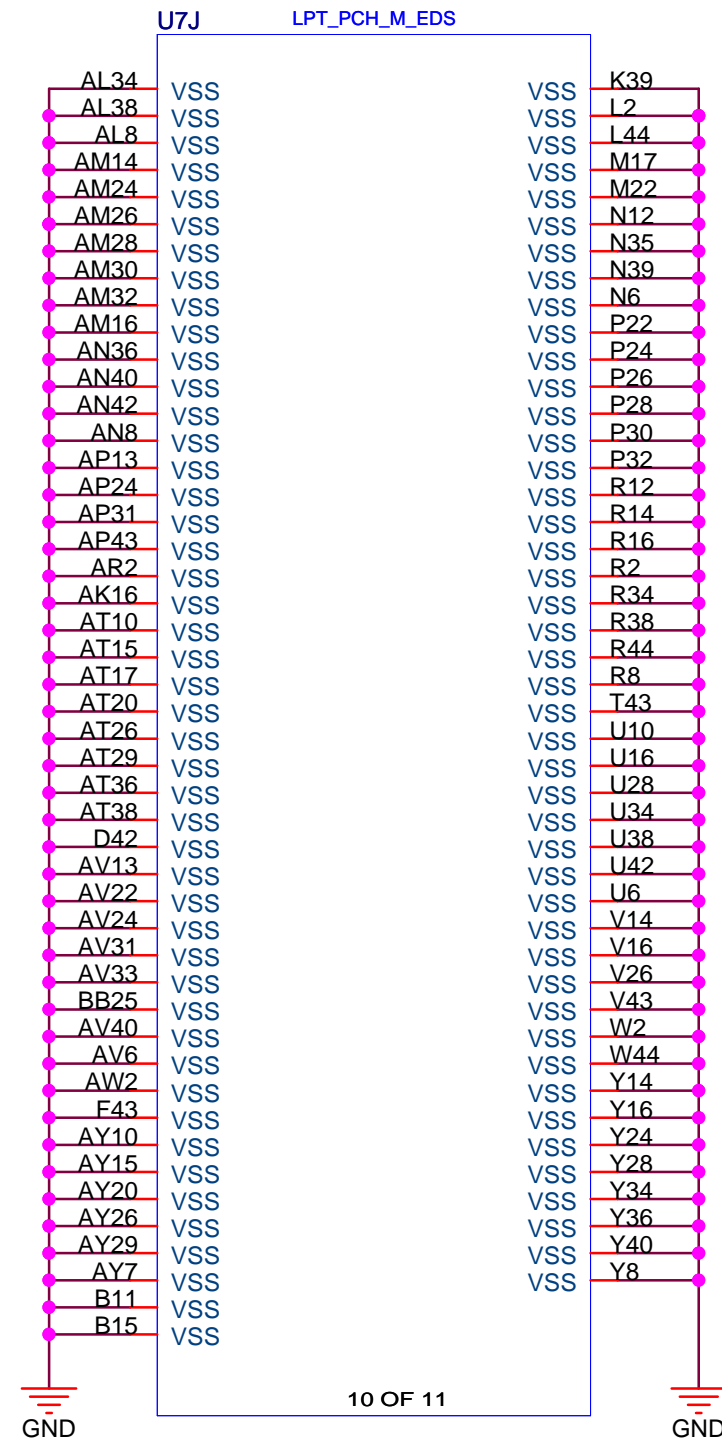
Lynx Point (Power)



Lynx Point (Power)



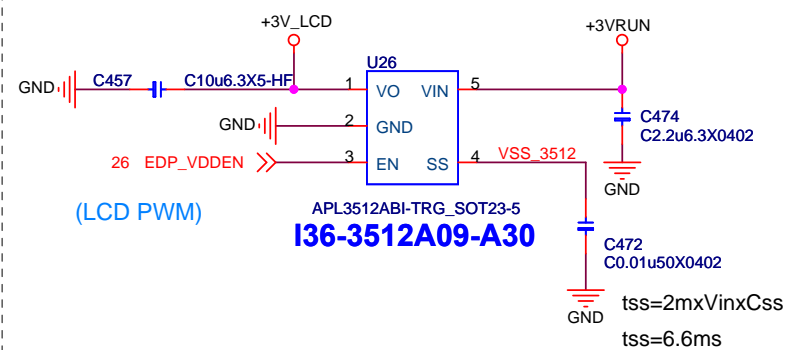
Lynx Point (GND)



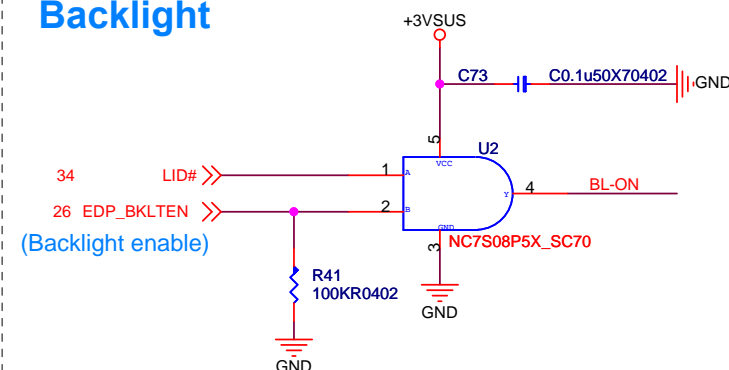
MICRO-STAR INT'L CO.,LTD.

Title		
PCH-8 (GND)		
Size	Document Number	Rev
	MS-16H3	0A
Date:	Monday, March 31, 2014	Sheet 31 of 69

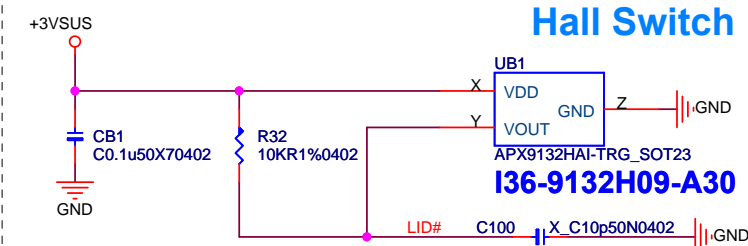
Pannel Device Logic Power



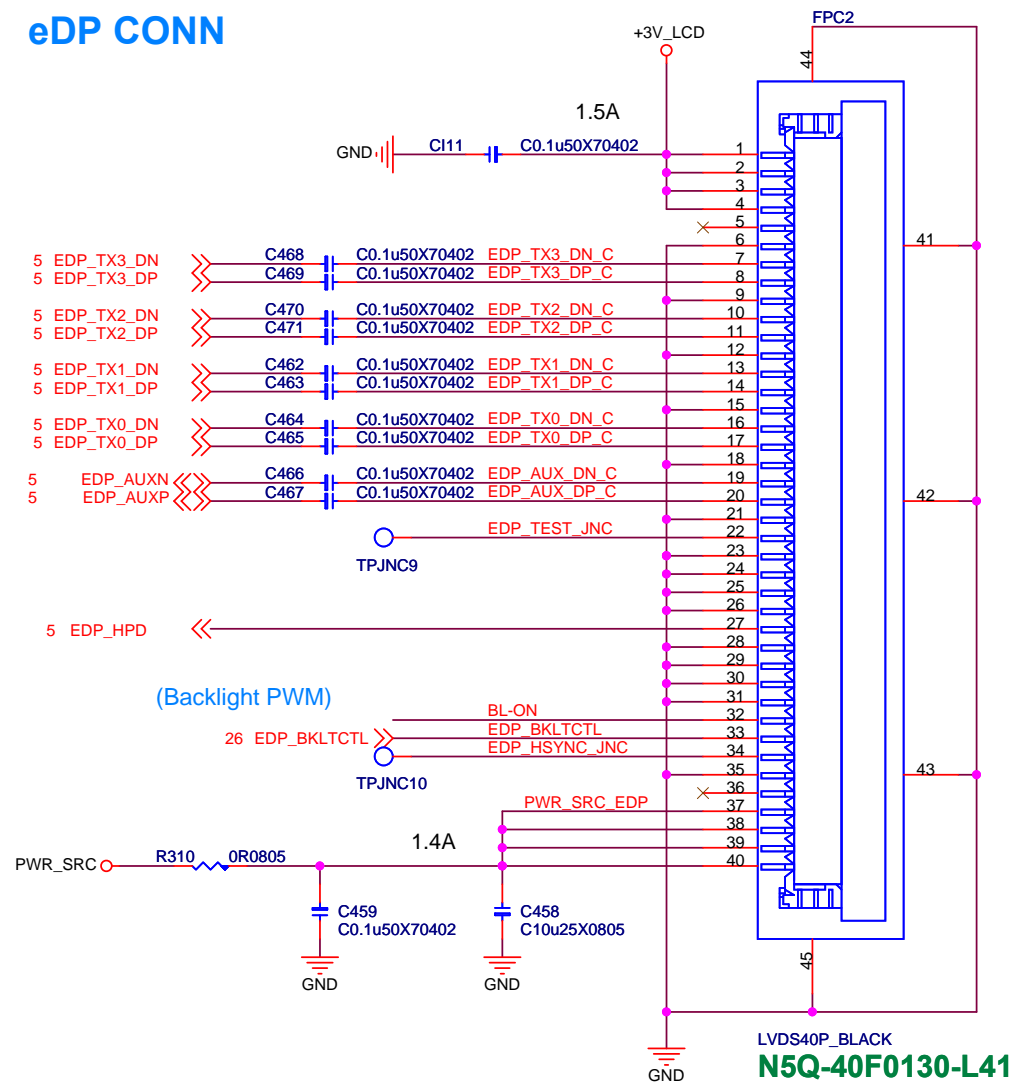
Backlight



Hall Switch



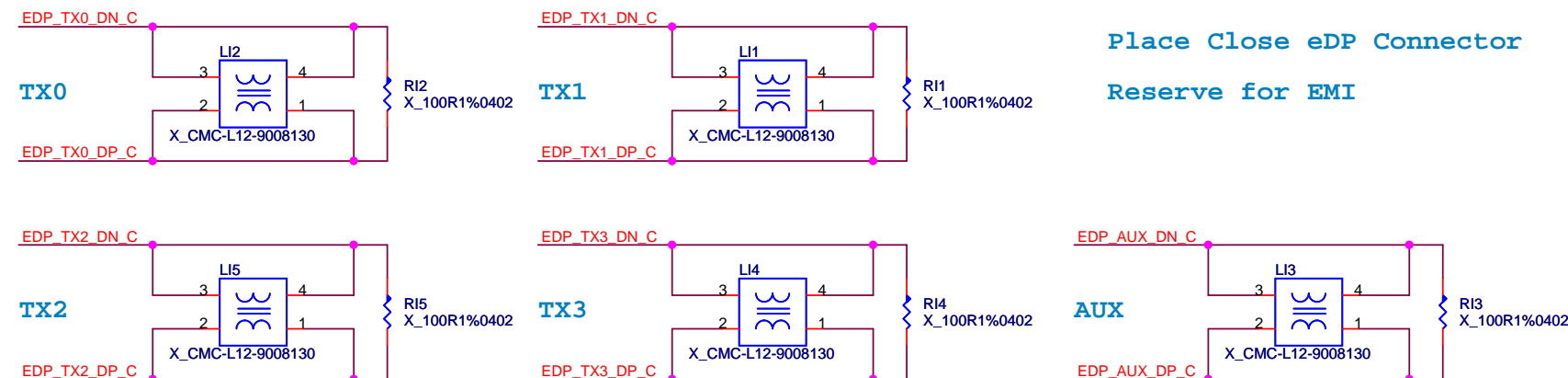
eDP CONN



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDP	HPDP signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

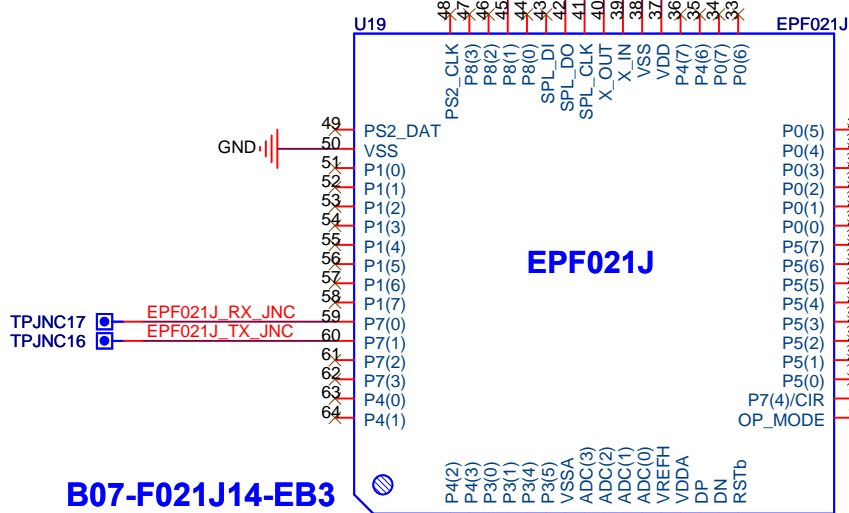
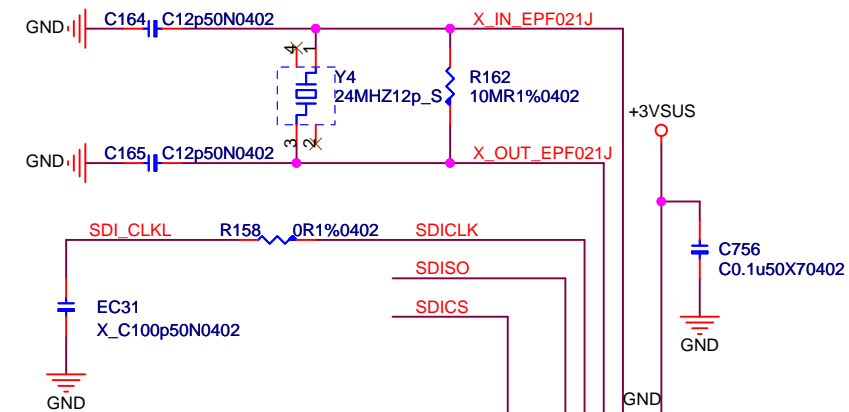
Place Close eDP Connector
Reserve for EMI



msi MICRO-STAR INT'L CO.,LTD.

Title	eDP switch & Conn/CAM/Lid		
Size	Document Number	Rev	0A
Custom	MS-16H3		
Date:	Monday, March 31, 2014	Sheet	32 of 69

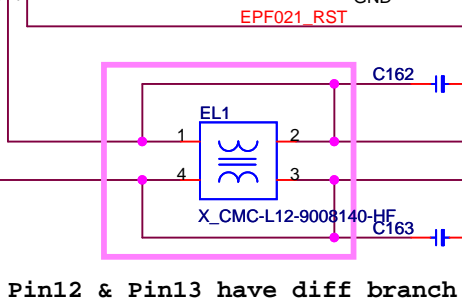
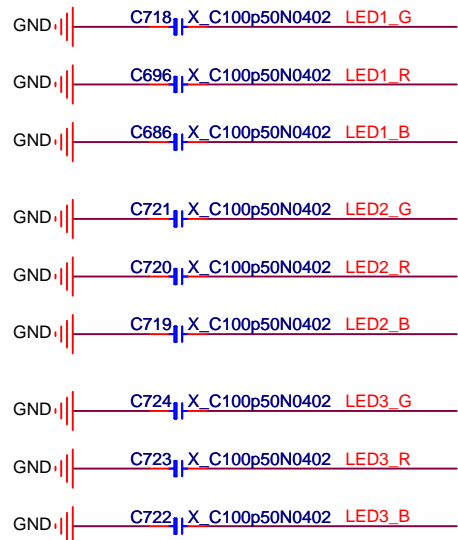
LED 8051 Controller



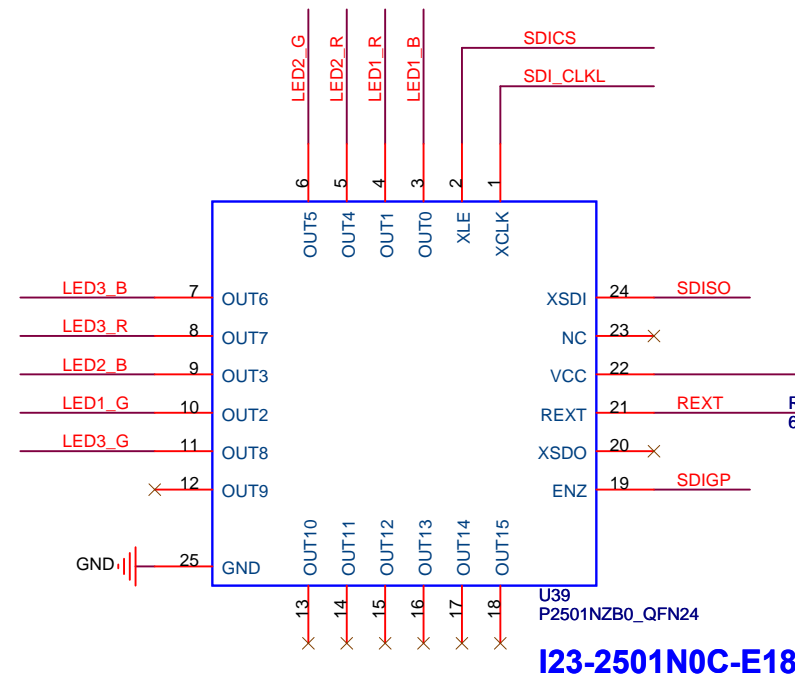
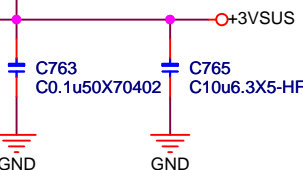
B07-F021J14-EB3

34,47 BATCLK_M
34,47 BATDATA_M

EMI



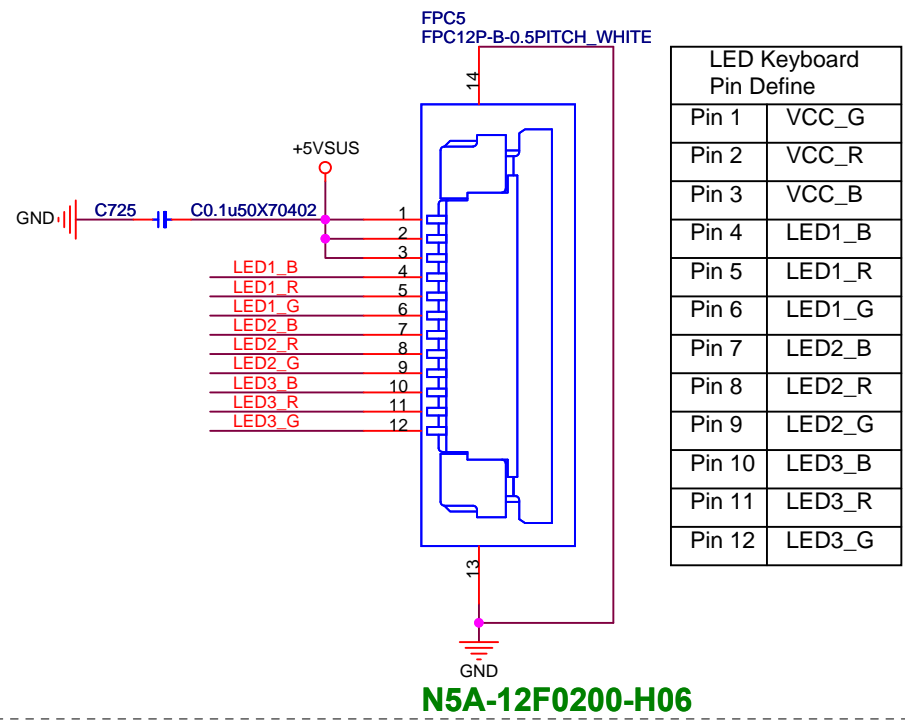
Pin12 & Pin13 have diff branch



Vcc=5V, output current 5-60mA
Vcc=3V, output current 2-45mA

I23-2501N0C-E18

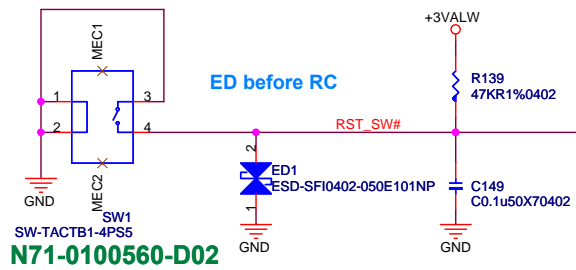
LED Keyboard CONN



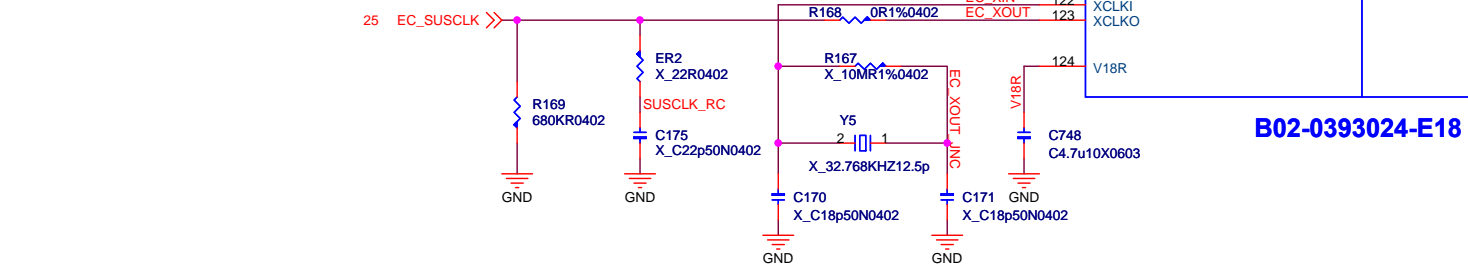
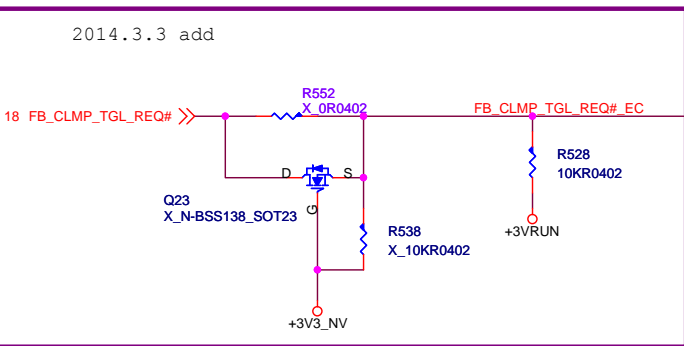
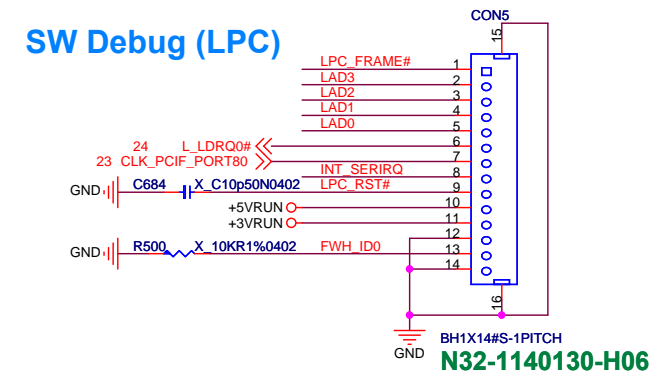
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

KBC(KB3930QFB1)

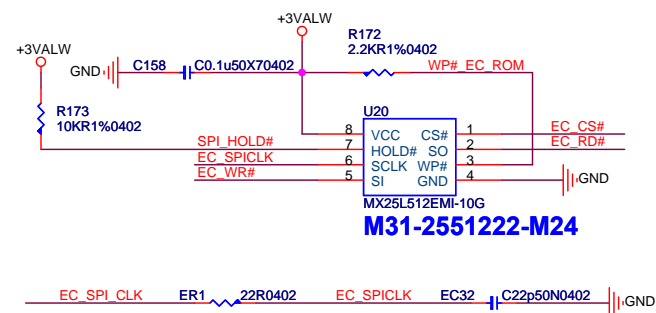
Hardware Reset



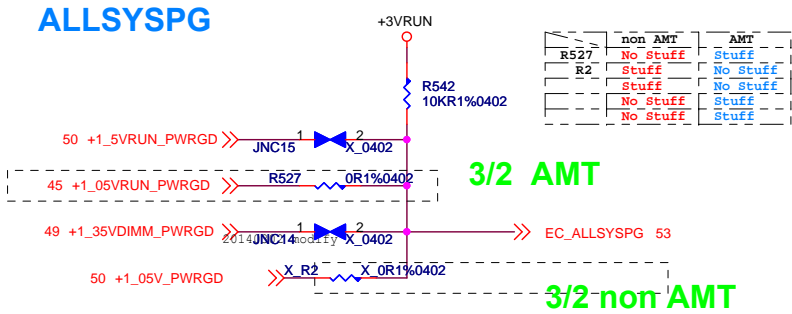
SW Debug (LPC)



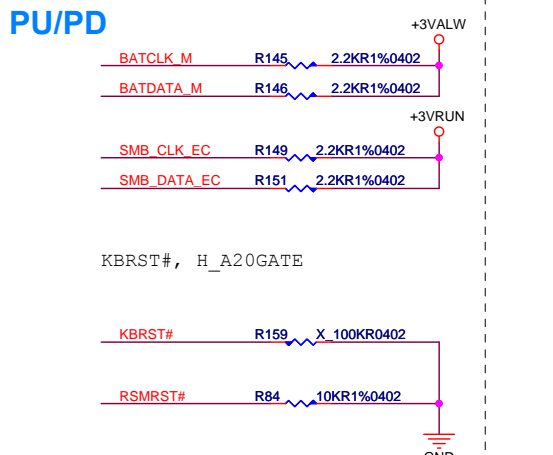
ROM



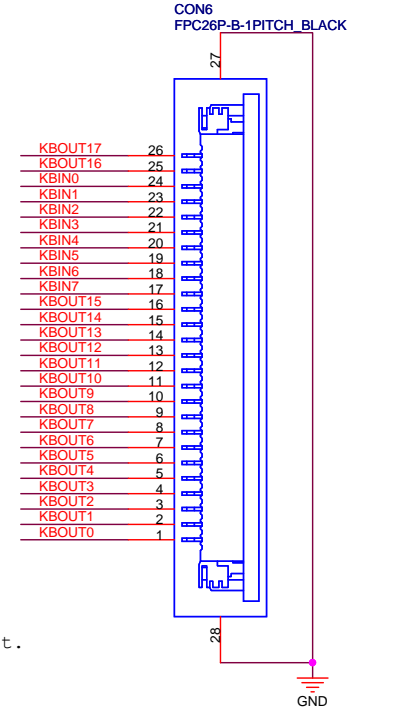
ALLSYSPG



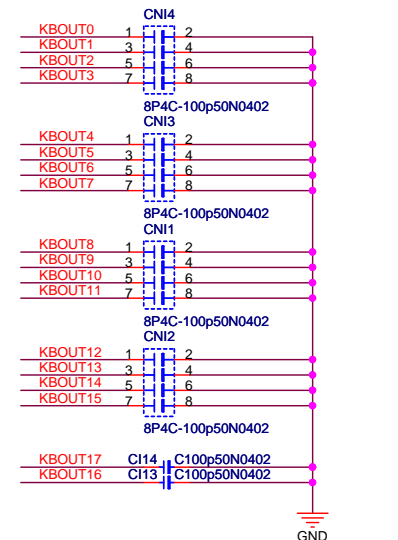
PU/PD



Keyboard conn

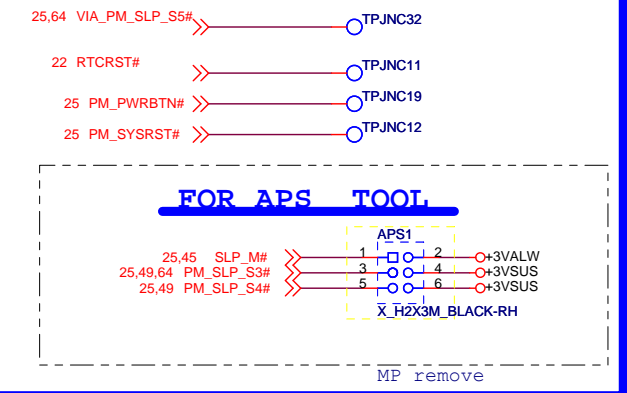


N5A-26F0340-H06

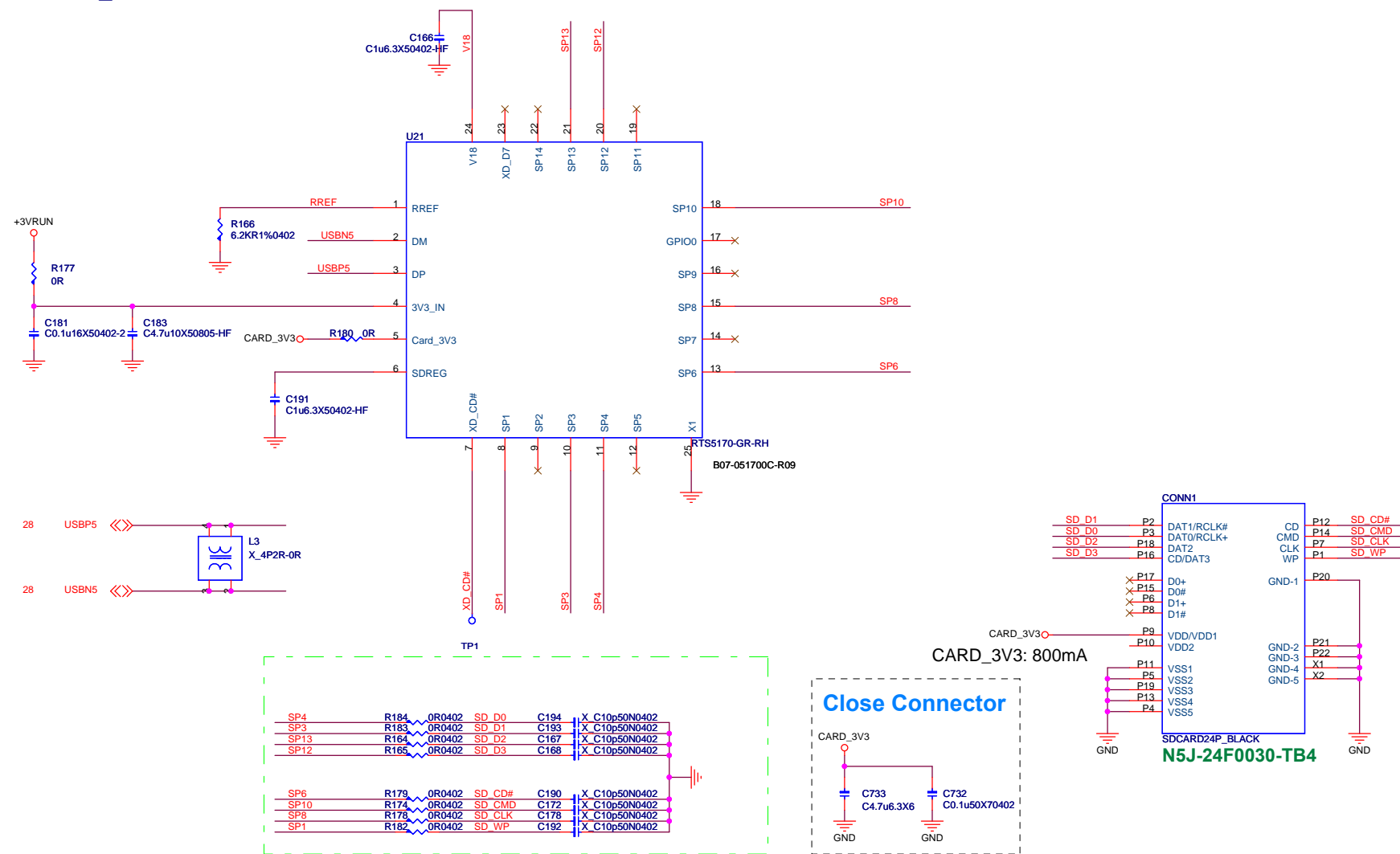


FLASH/ME DEBUG MODE STRAP

20140311 add



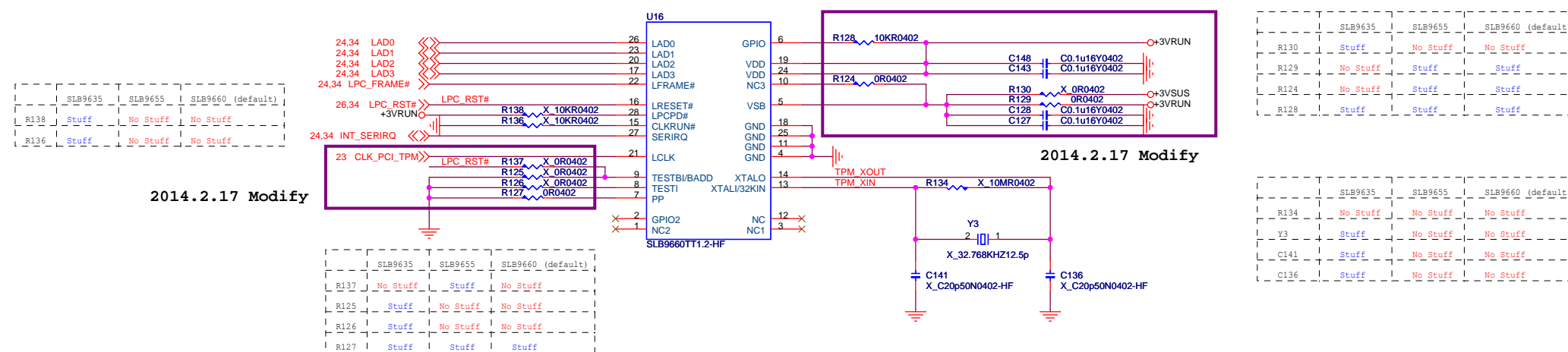
CARD READER_RTS5170



For EMI and Close to RTS5170

Pin#	Name	I/O Type	Description
1	RREF	I	Connect external resistor (6.2K \pm 1%) to reference ground
2	DM	I/O	USB D- signal
3	DP	I/O	USB D+ signal
4	3V3_IN	I	3.3V power input
5	CARD_3V3	O	3.3V power for all cards
6	SDREG	O	Internal regulator for SD card. An external capacitor should be connected
7	XD_CD#	I	xD Card Detect (xD_CD#)
8	SP1	I/O	xD Ready Signal (xD_RDY), SD Write Protect (SD_WP) and MS Clock (MS_CLK)
9	SP2	I/O	xD RE# and MS Card Detect (MS_INS#)
10	SP3	I/O	xD CE# and SD Data 1 (SD_DAT1)
11	SP4	I/O	xD_CLE, SD Data 0 (SD_DAT0) and MS Data 7 (MS_D7)
12	SP5	I/O	xD_ALE, SD Data 7 (SD_DAT7) and MS Data 3 (MS_D3)
13	SP6	I/O	xD_WE# and SD Card Detect (SD_CD#)
14	SP7	I/O	xD Write Protect (xD_WP), SD_Data 6 (SD_DAT6) and MS Data 6 (MS_D6)
15	SP8	I/O	xD Data 0 (xD_D0), SD Clock (SD_CLK) and MS Data 2 (MS_D2)
16	SP9	I/O	xD Data 1 (xD_D1), SD Data 5 (SD_D5) and MS Data 0 (MS_D0)
17	GPIO0	I/O	General purpose input/output with interrupt ability
18	SP10	I/O	xD Data 2 (xD_D2) and SD command signal (SD_CMD)
19	SP11	I/O	xD Data 3 (xD_D3), SD Data 4 (SD_DAT4) and MS Data 4 (MS_D4)
20	SP12	I/O	xD Data 4 (xD_D4), SD Data 3 (SD_DAT3) and MS Data 1 (MS_D1)
21	SP13	I/O	xD Data 5 (xD_D5), SD Data 2 (SD_DAT2) and MS Data 5 (MS_D5)
22	SP14	I/O	xD Data 6 (xD_D6) and MS BS
23	XD_D7	I/O	xD Data 7 (xD_D7)
24	V18	O	Regulated supply voltage (1.8V \pm 10%) from internal 3.3V to 1.8V regulator; supplies internal digital circuits. An external capacitance should be connected

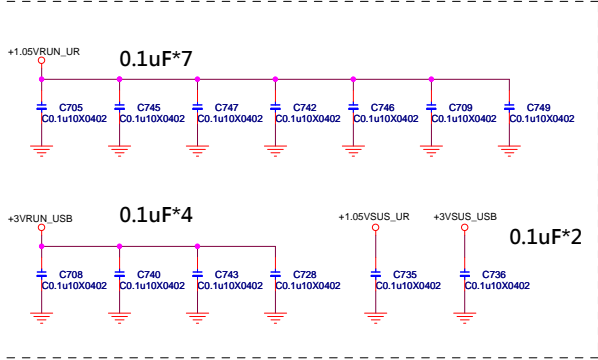
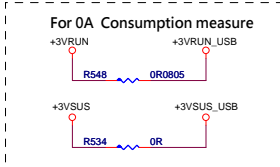
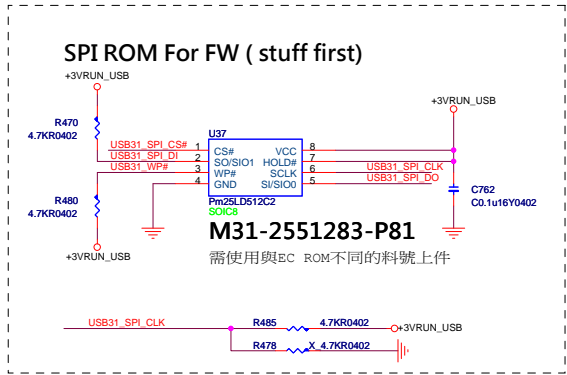
TPM



USB 3.0 / iCharger

USB3.0 CNT-1

USB3.0 Port-5
USB2.0 Port-8

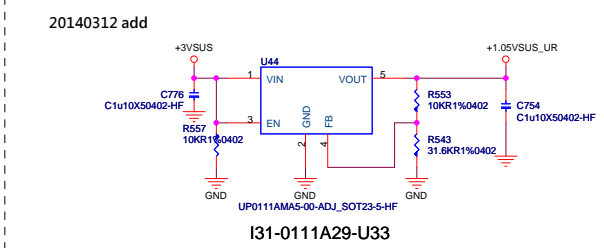
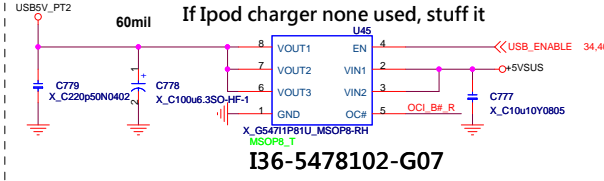
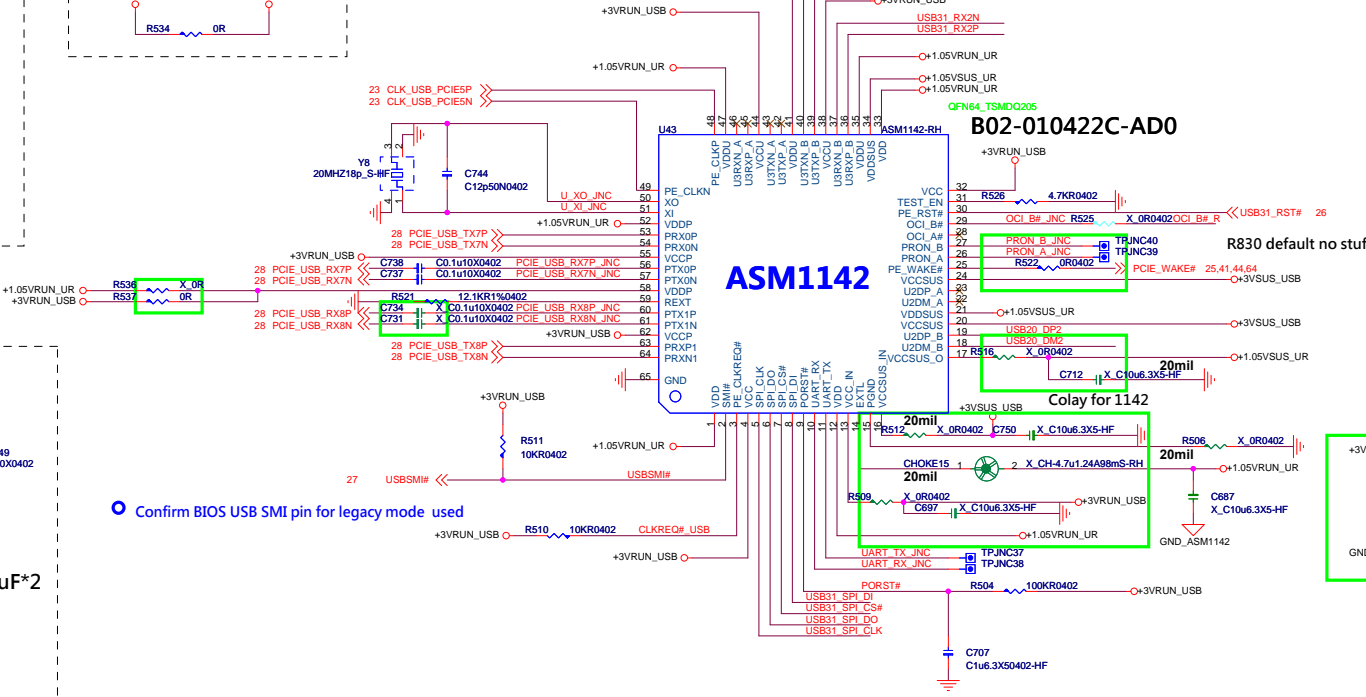


Confirm BIOS USB SMI pin for legacy mode used

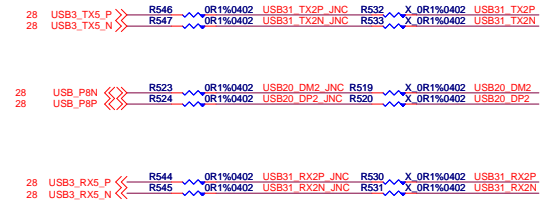


Confirm BIOS USB SMI pin for legacy mode used

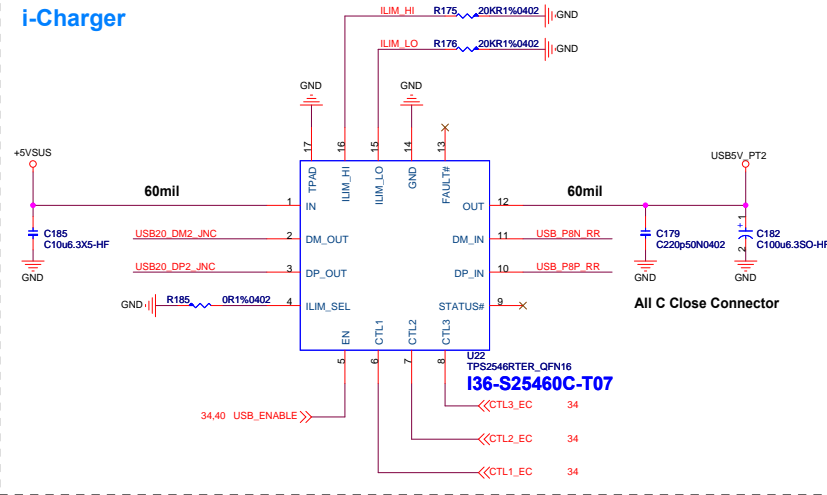
PCIE to USB 3.1



USB 3.1 Port 1

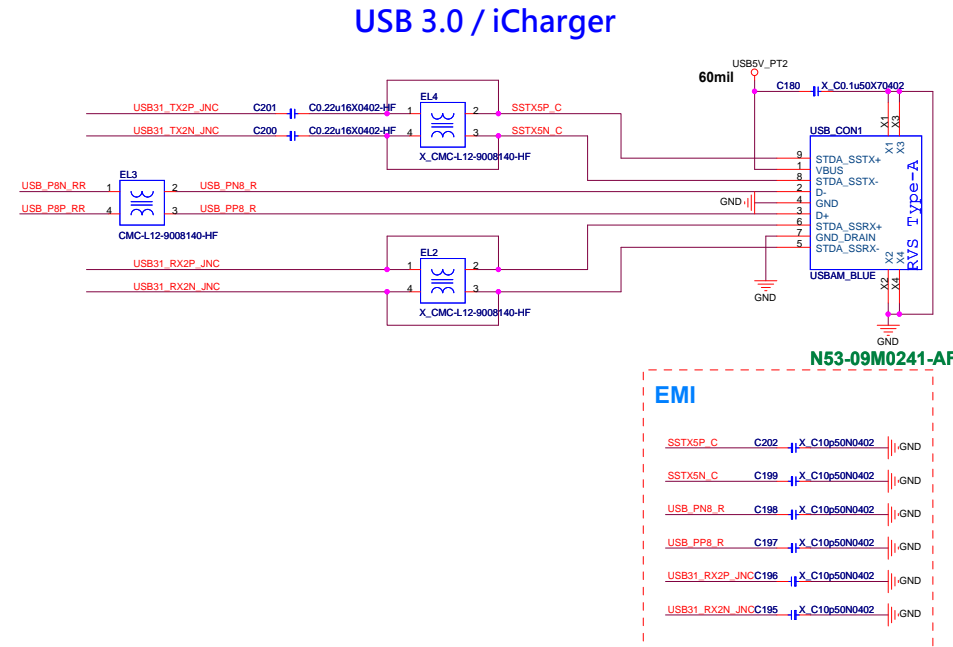


i-Charger

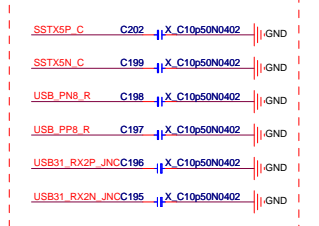


USB3.0 CNT-1

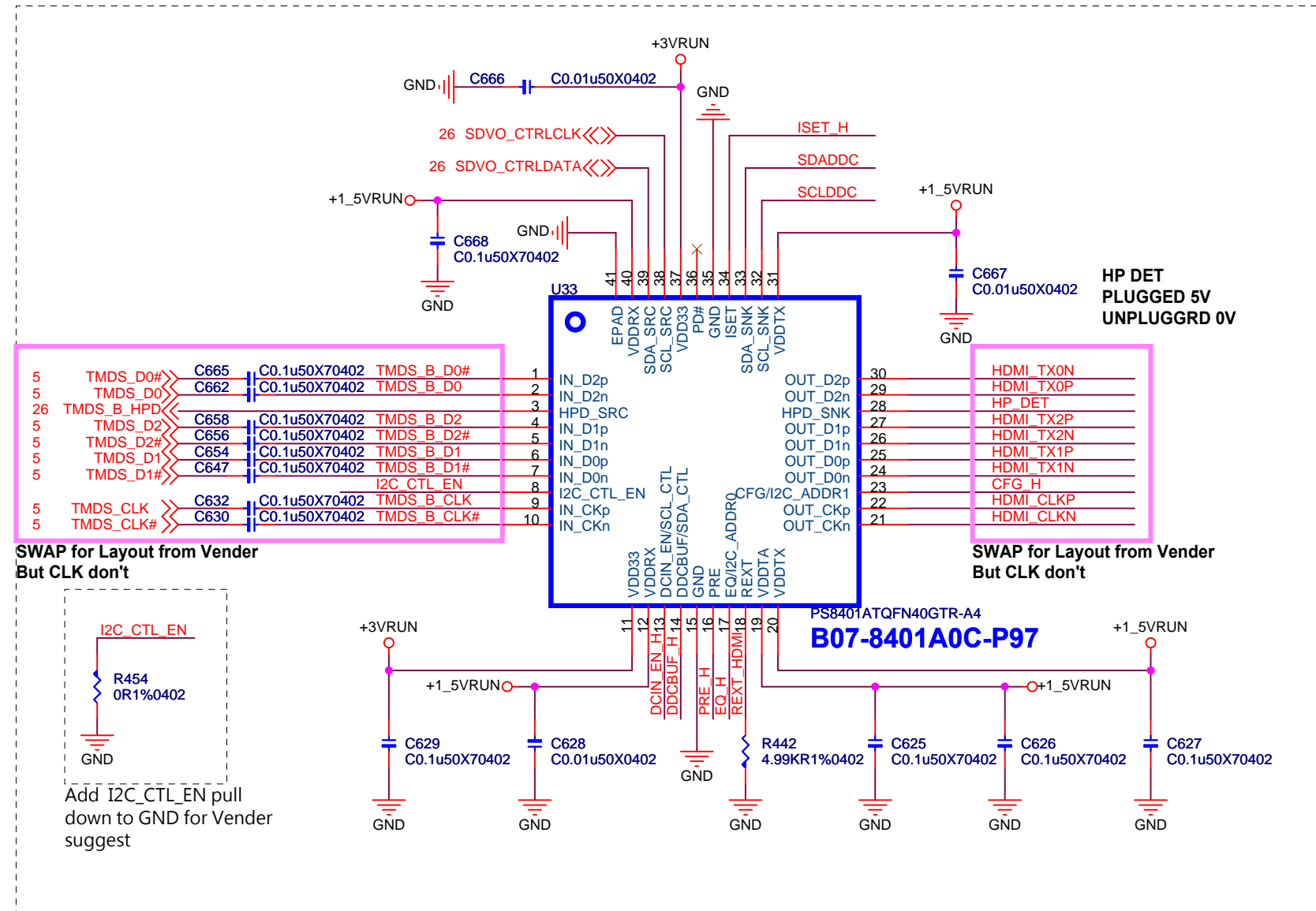
USB3.0 Port-6
USB2.0 Port-9



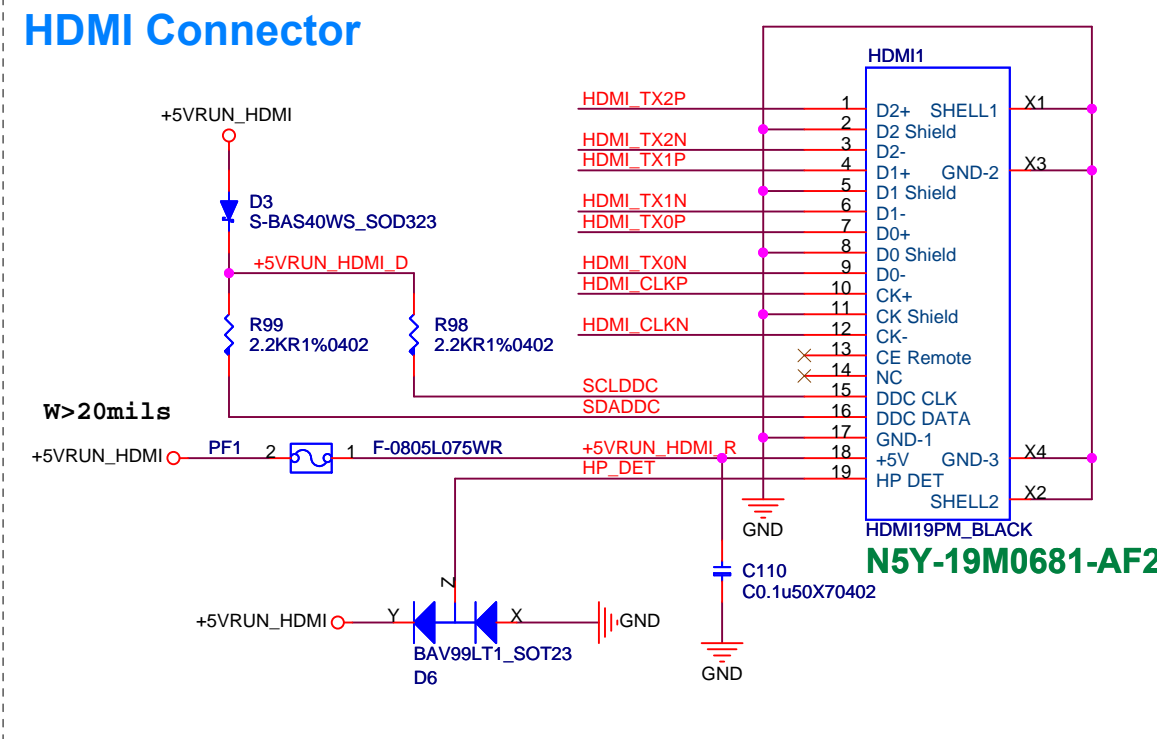
EMI



HDMI Repeater



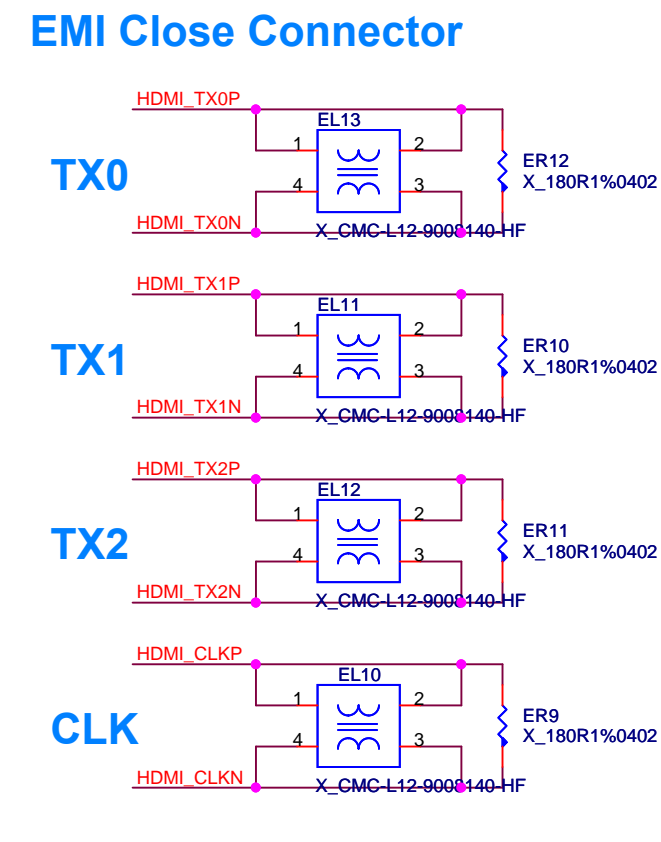
HDMI Connector



An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

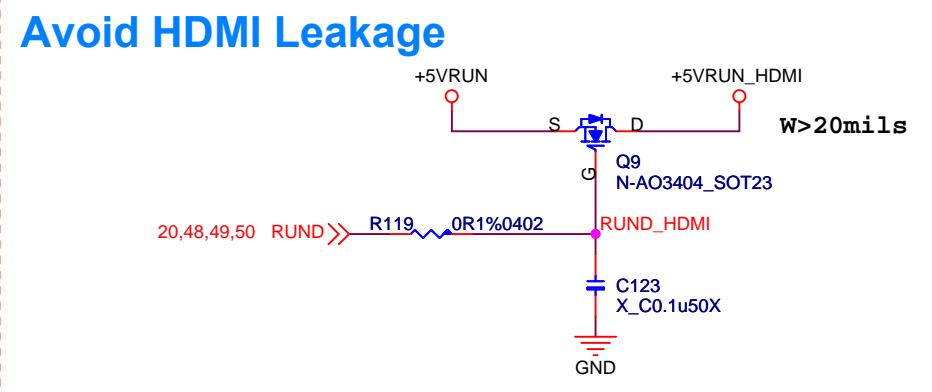
HPD_SNK Internal PD 150kohm

EMI Close Connector

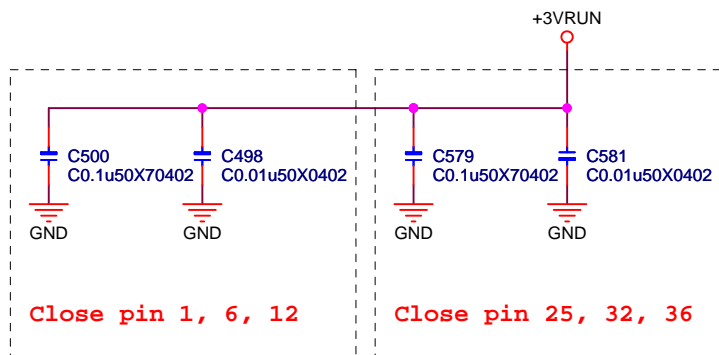
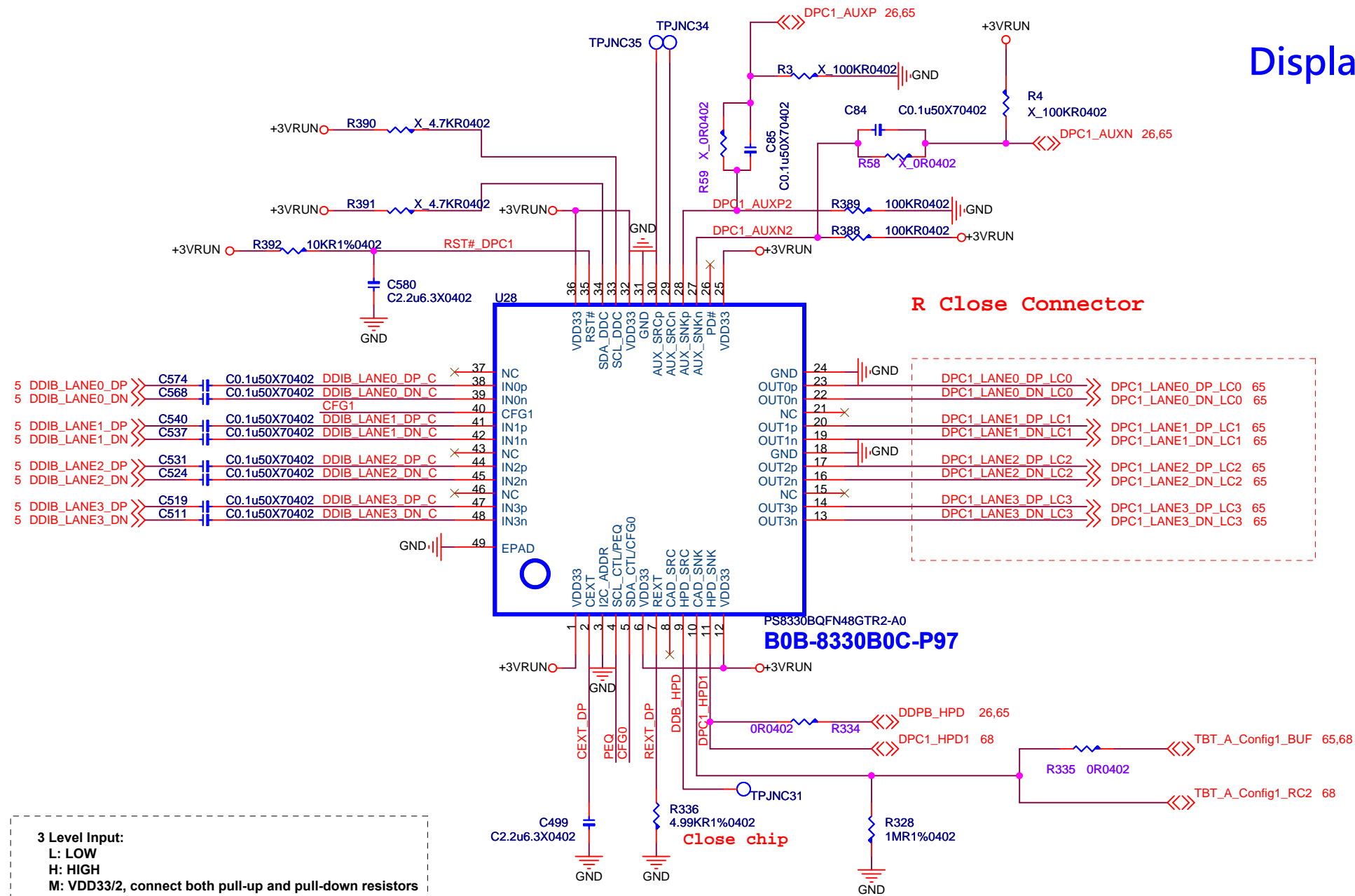


ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

Avoid HDMI Leakage

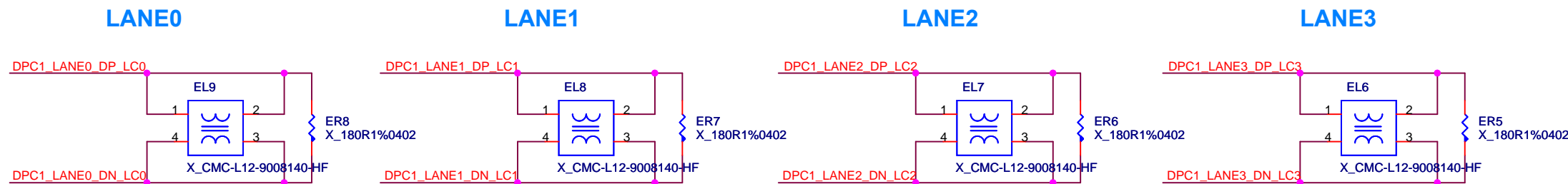


Display Port

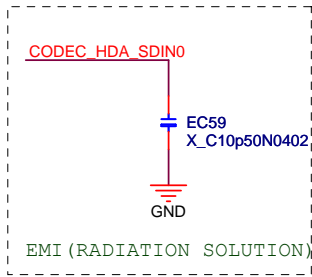
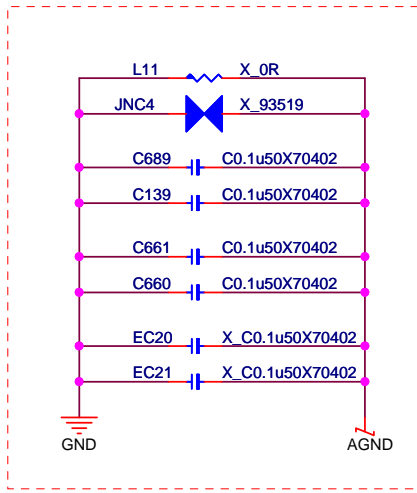


CAD_SNK Have internal Pull down 1Mohm.
HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

EMI Close Connector



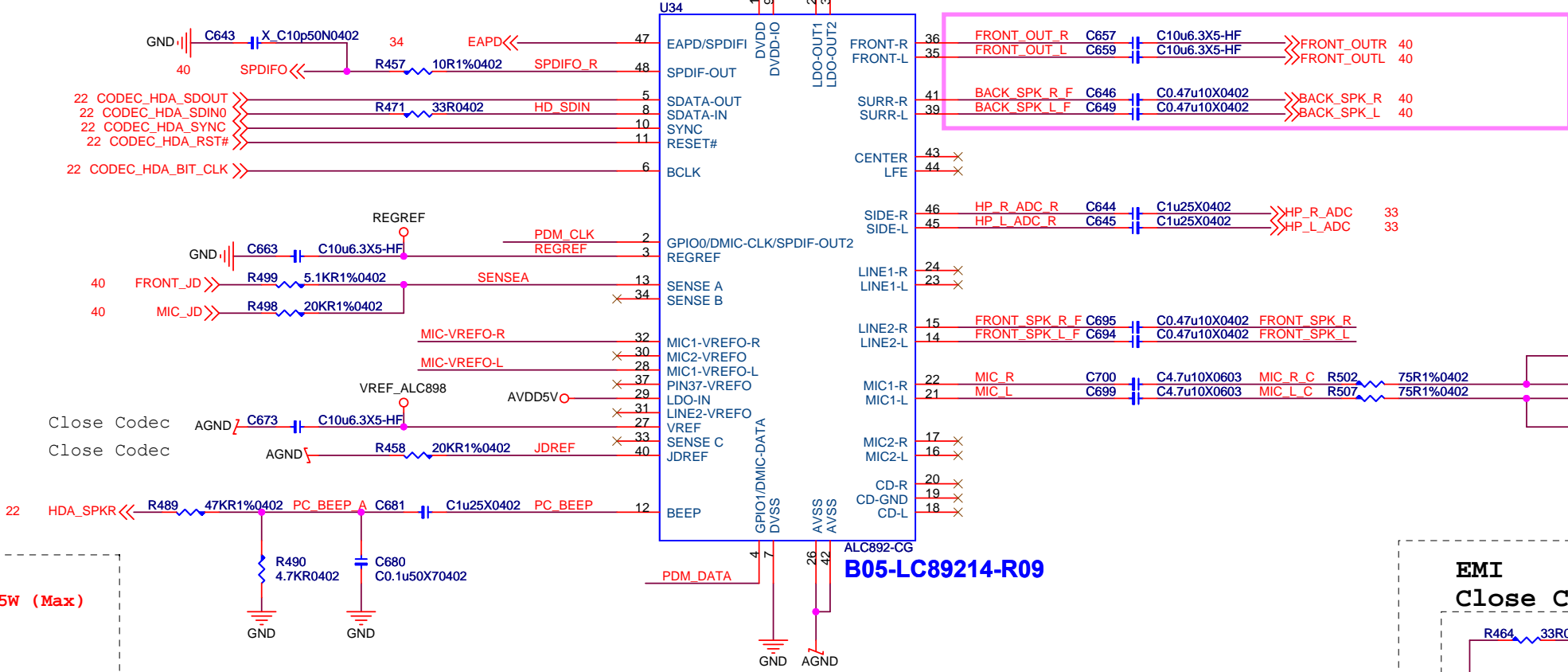
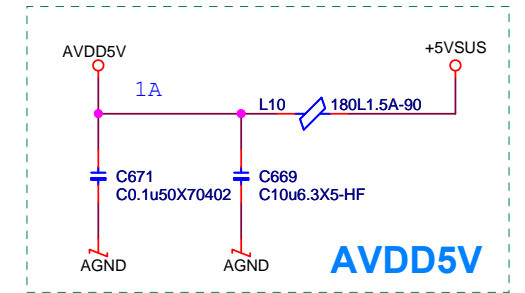
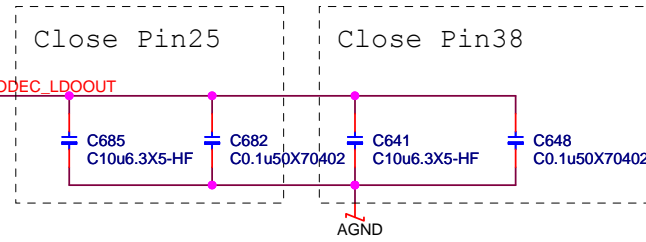
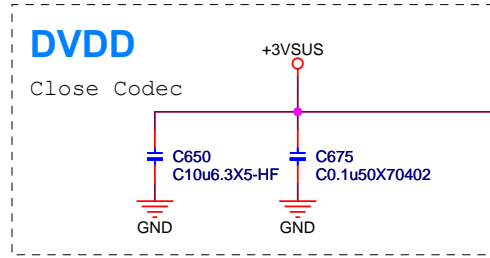
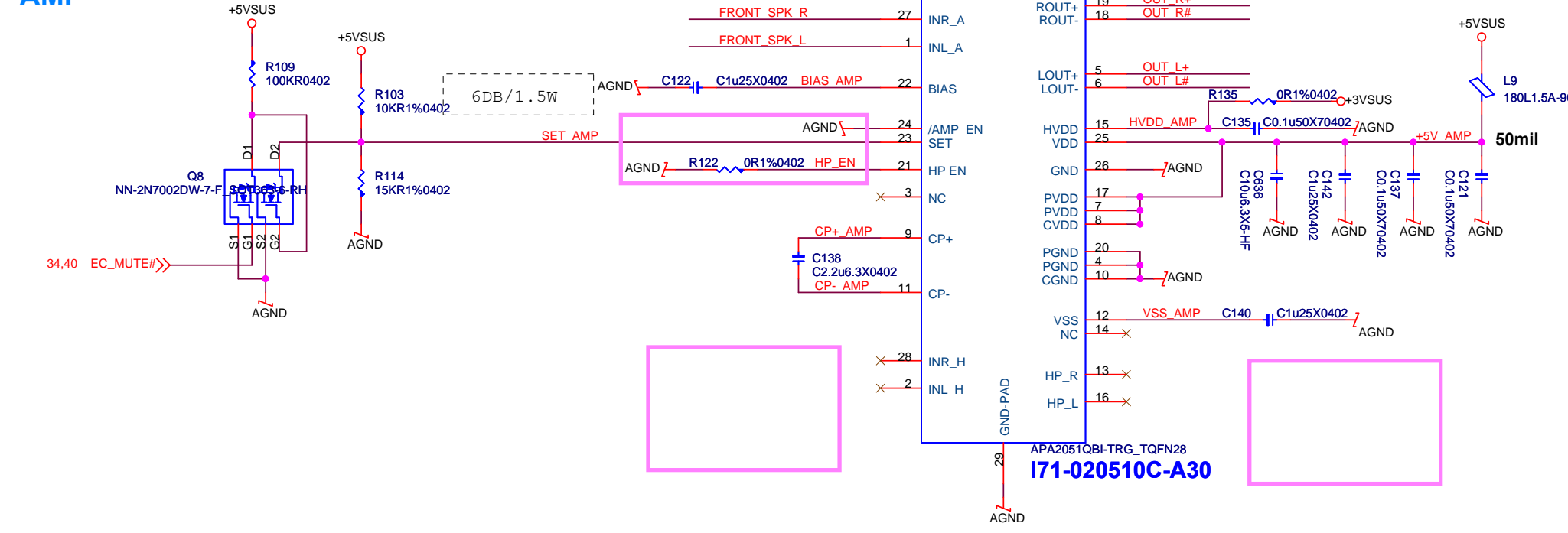
Audio CODEC/Audio AMP



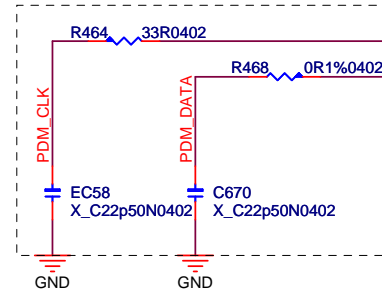
APA2051 Pin23: Gain Setting
Speaker Spec: 2.0W(Normal), 2.5W (Max)
 $V_o = (2 \times 4)^{0.5} = 2.828$
 $\text{dB} - 20\text{LOG}(V_o/V_i)$
Gain: $2.828\text{Vrms}/1.2\text{Vrms} = 2.36$
7dB $\approx 20\text{LOG } 2.36$
7dB : Setting Pin23 on 3.1V
(R103:13Kohm, R106:22Kohm)

For 6dB When Using 1.5W (Normal)
(R103:10Kohm, R106:15Kohm)

AMP



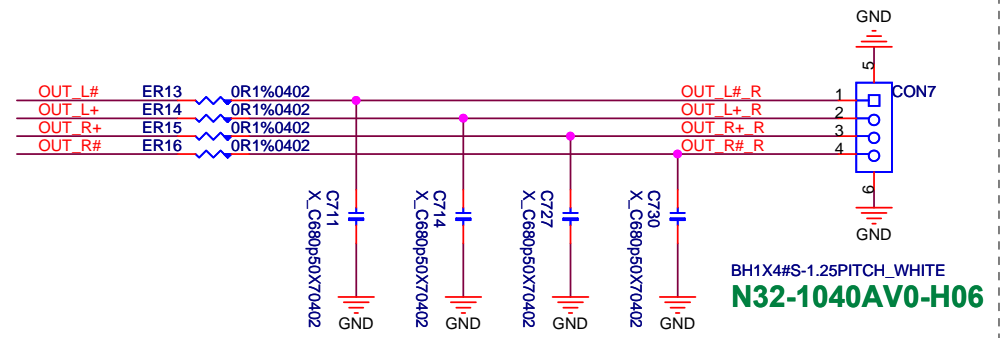
EMI Close Codec



Internal Mic



Internal Speaker Conn

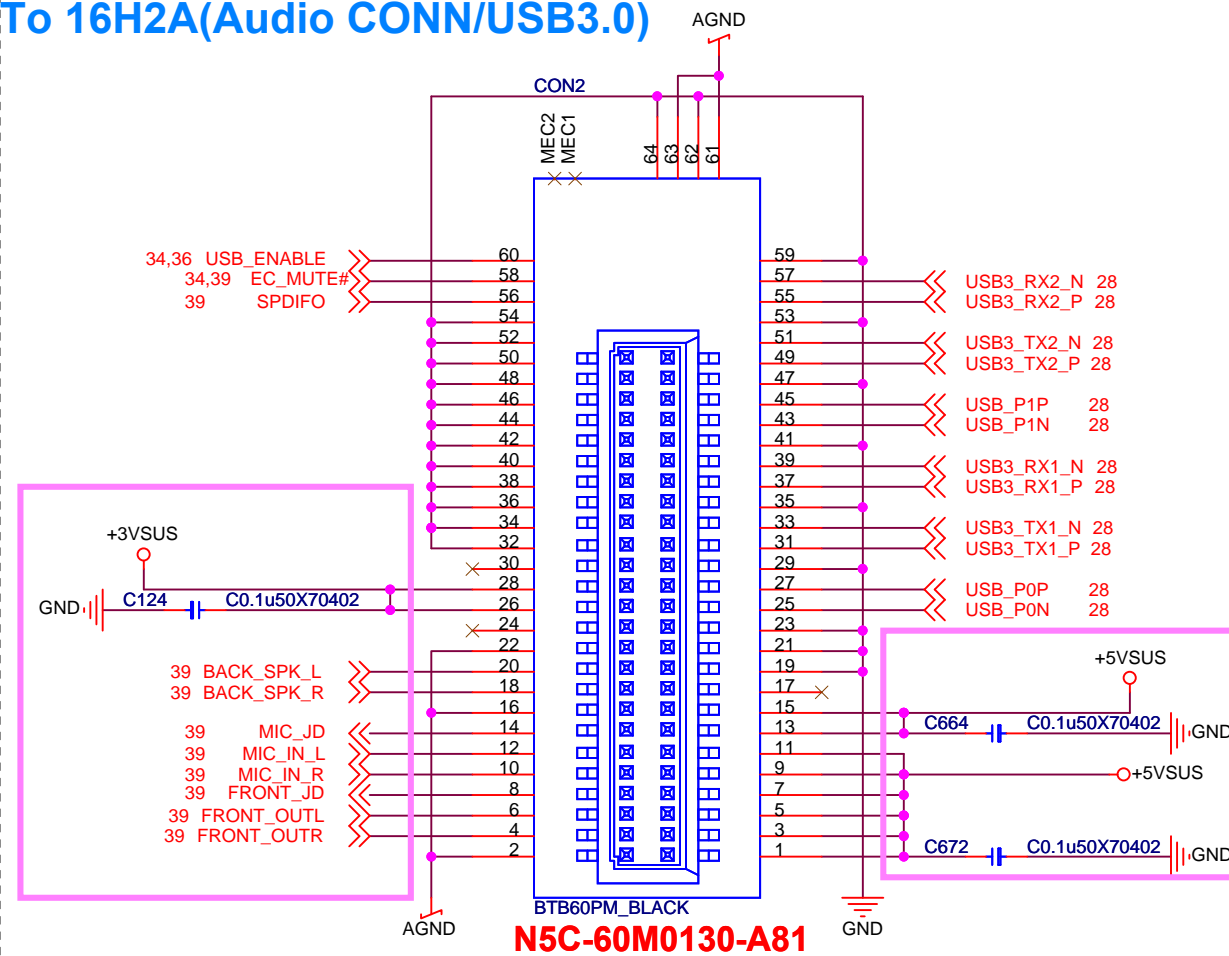


msi MICRO-STAR INT'L CO.,LTD.

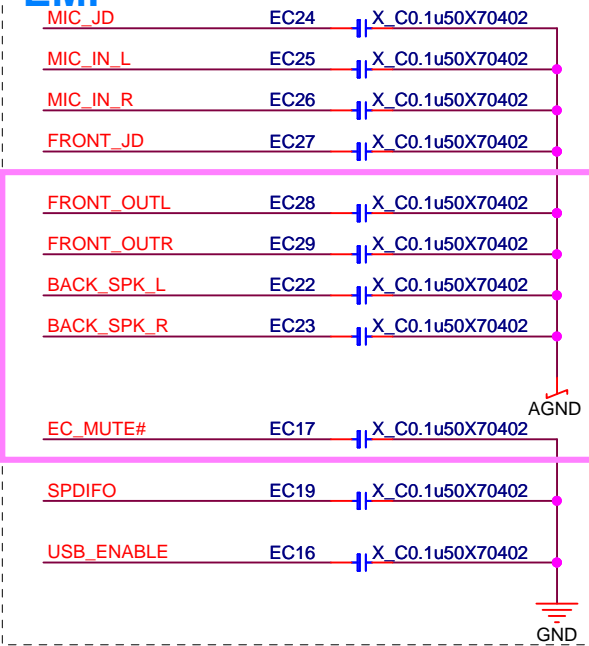
Title			Audio CODEC/Audio AMP
Size	Document Number	Rev	0A
MS-16H3			
Date:	Monday, March 31, 2014	Sheet	39 of 69

CPU FAN/BTB CONN

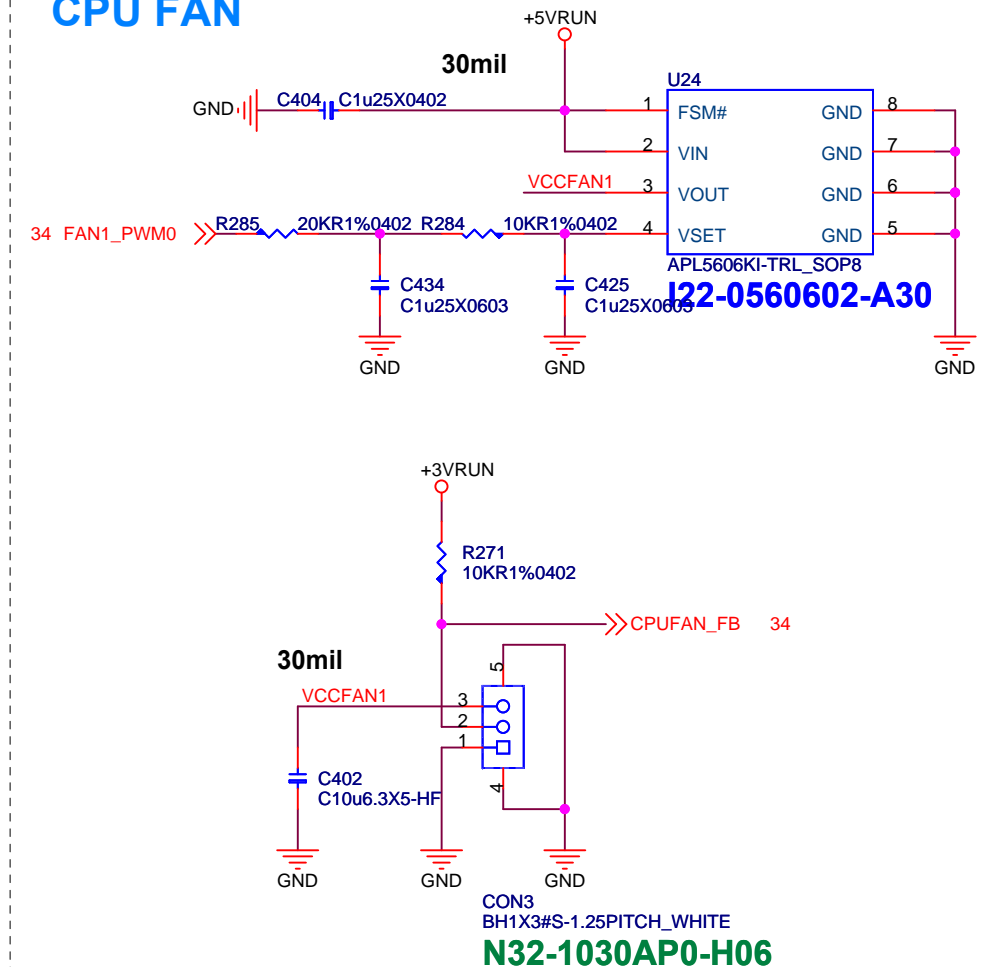
To 16H2A(Audio CONN/USB3.0)



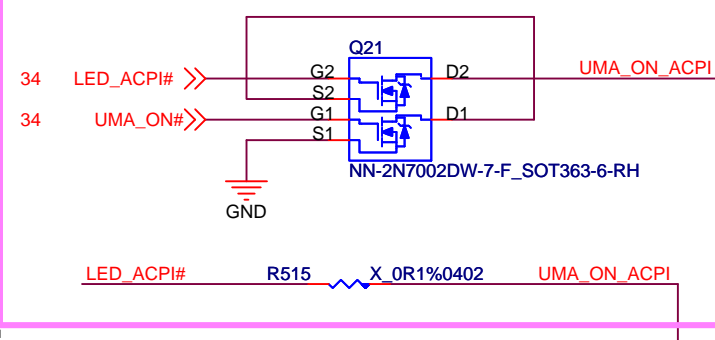
EMI



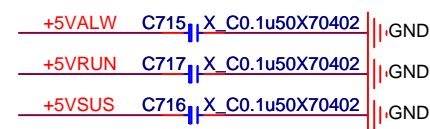
CPU FAN



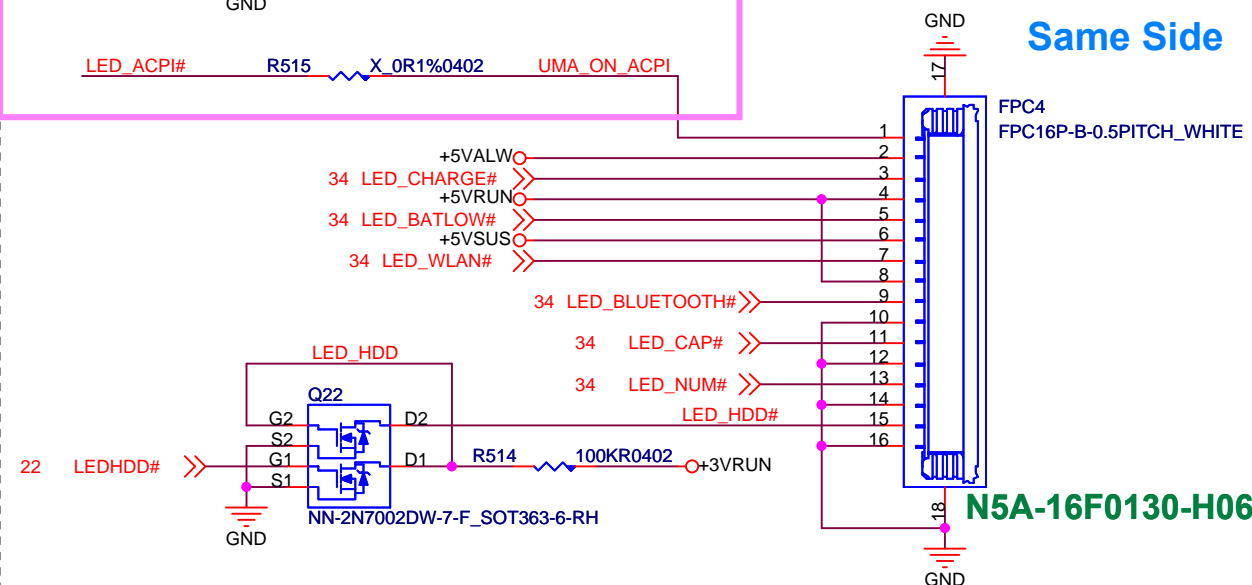
S3 Breath S0 No active



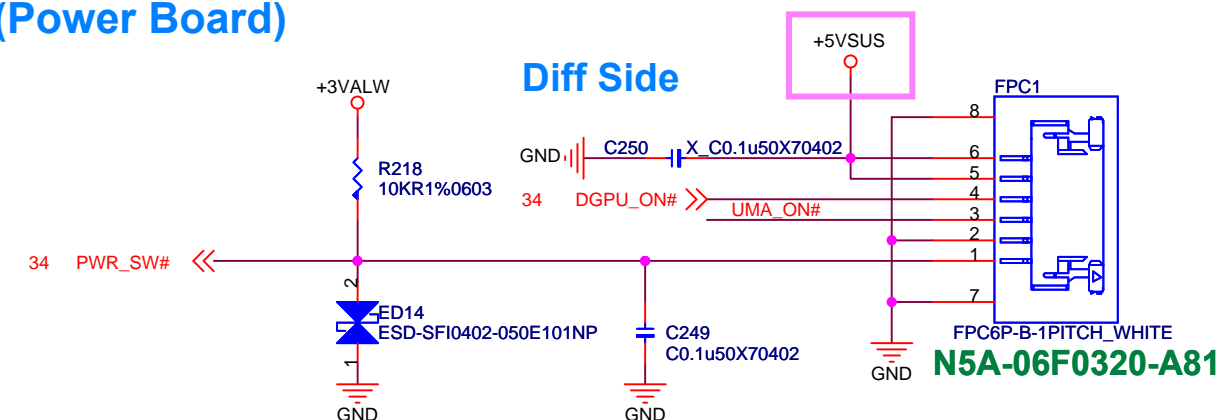
To 16H2B(LED Board)



Same Side



To 16H2C (Power Board)



msi

MICRO-STAR INT'L CO.,LTD.

Title
CPU FAN/BTB CONN

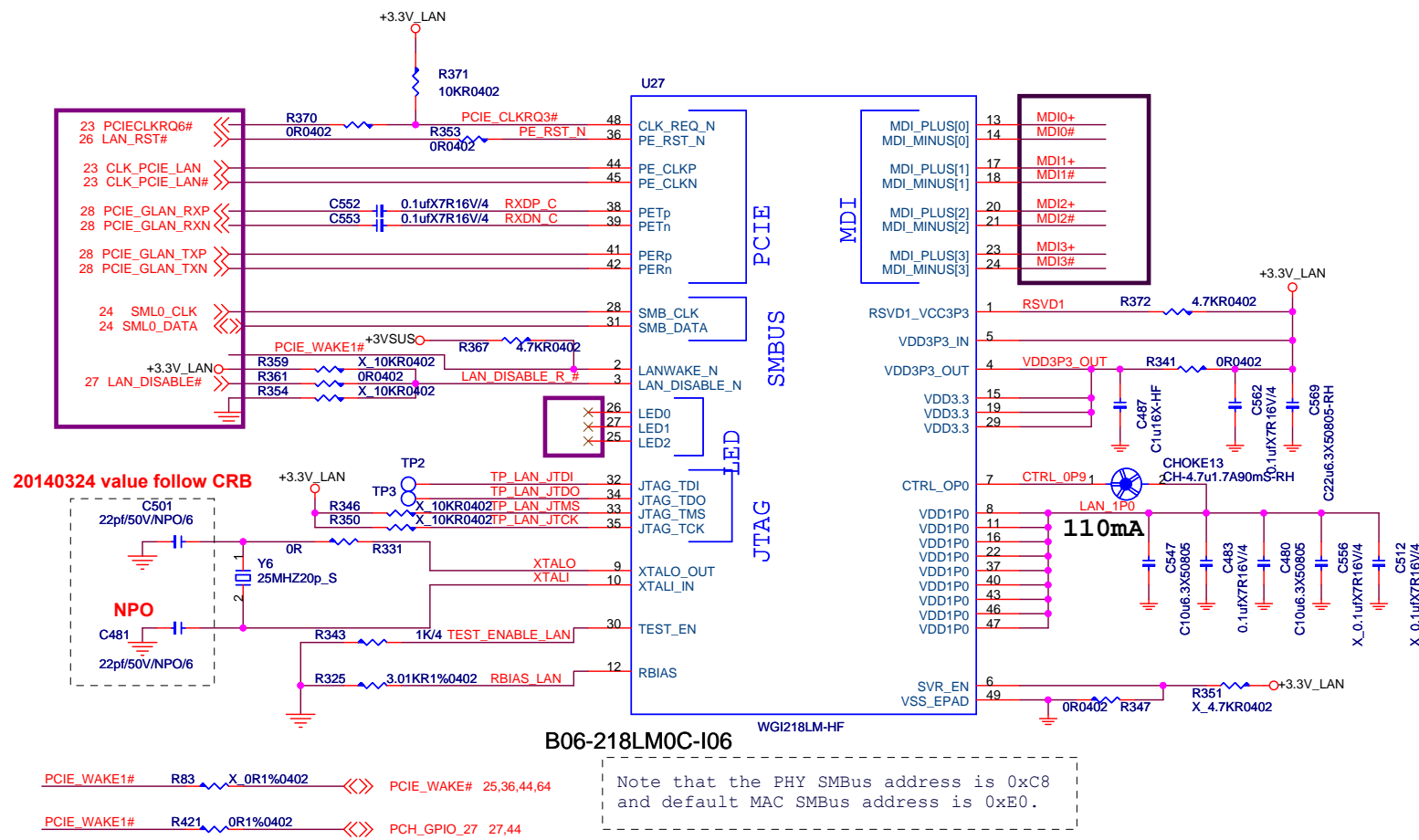
Size
Document Number
MS-16H3

Rev
0A

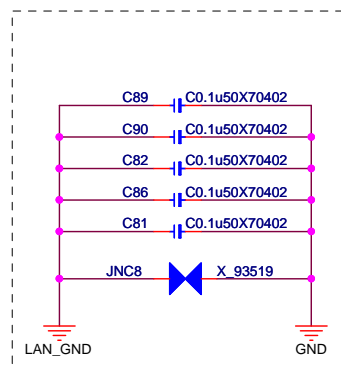
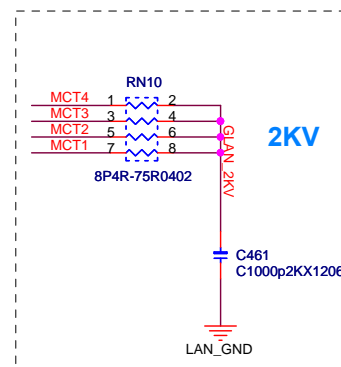
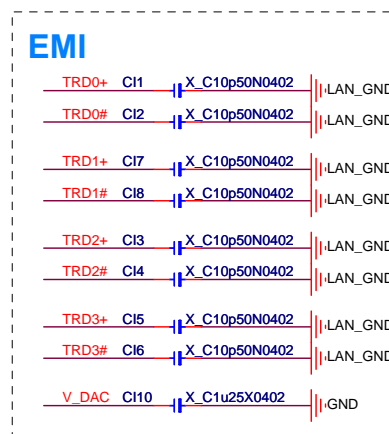
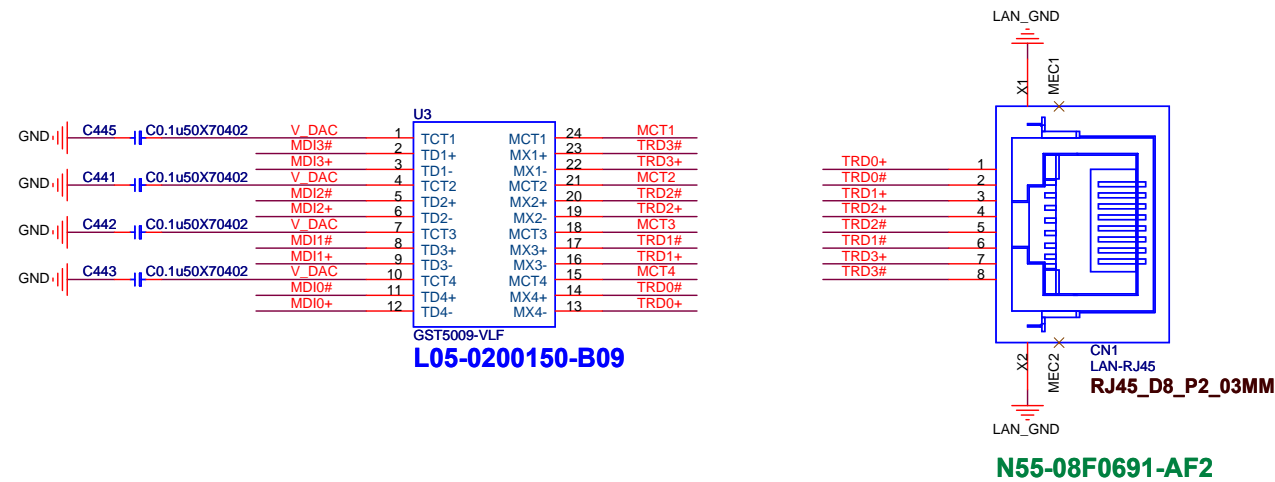
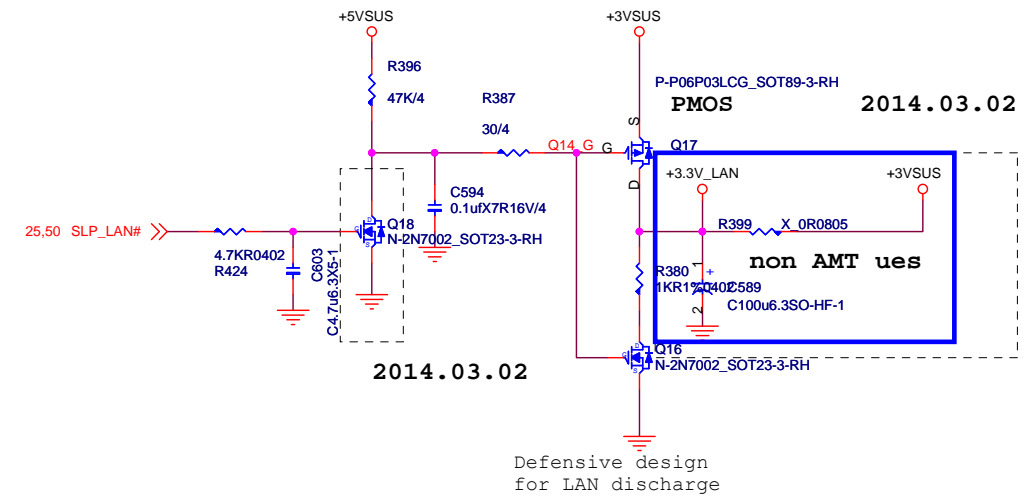
Date: Monday, March 31, 2014

Sheet 40 of 69

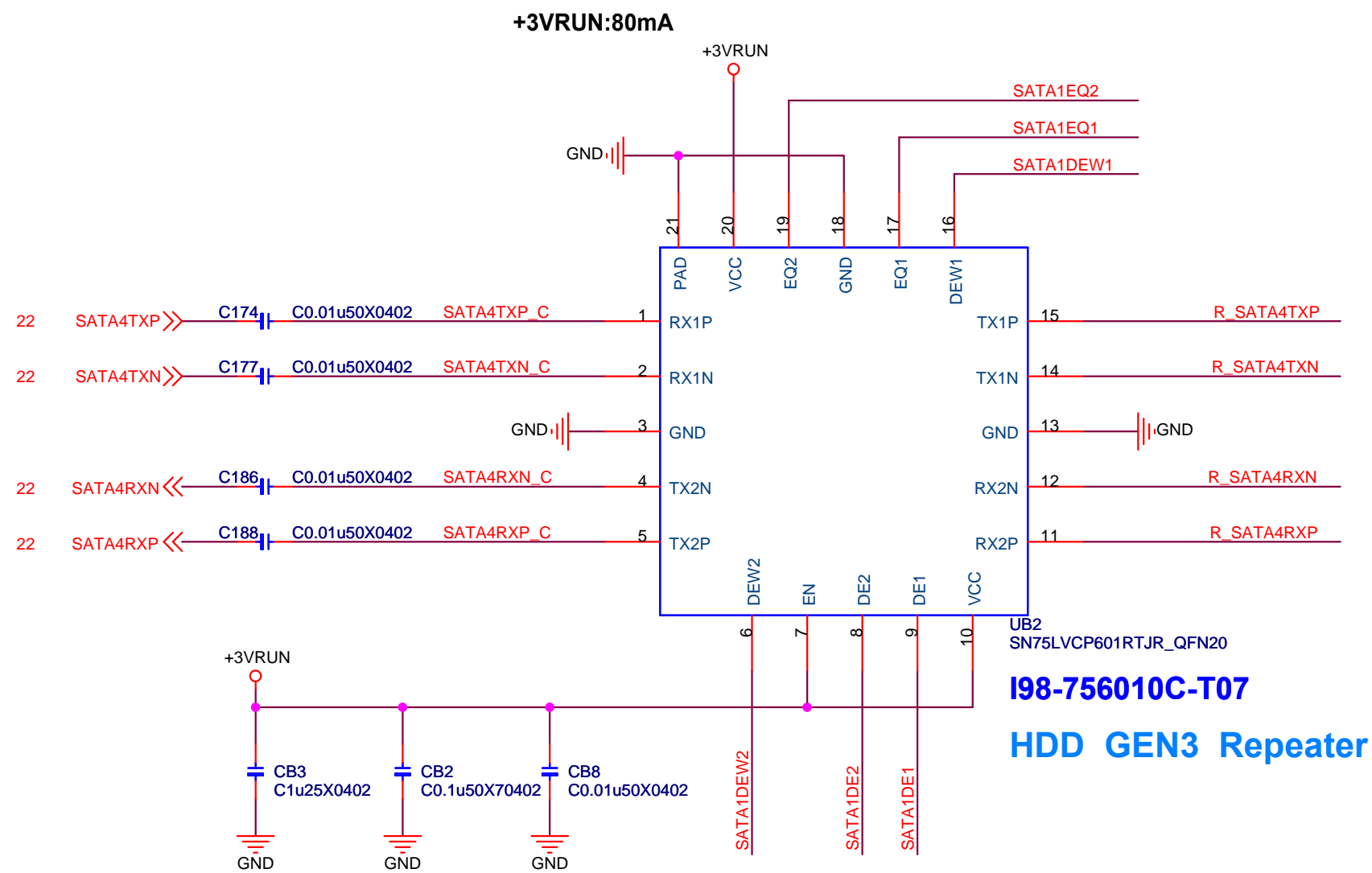
INTEL Clarkville LAN(I218LM)



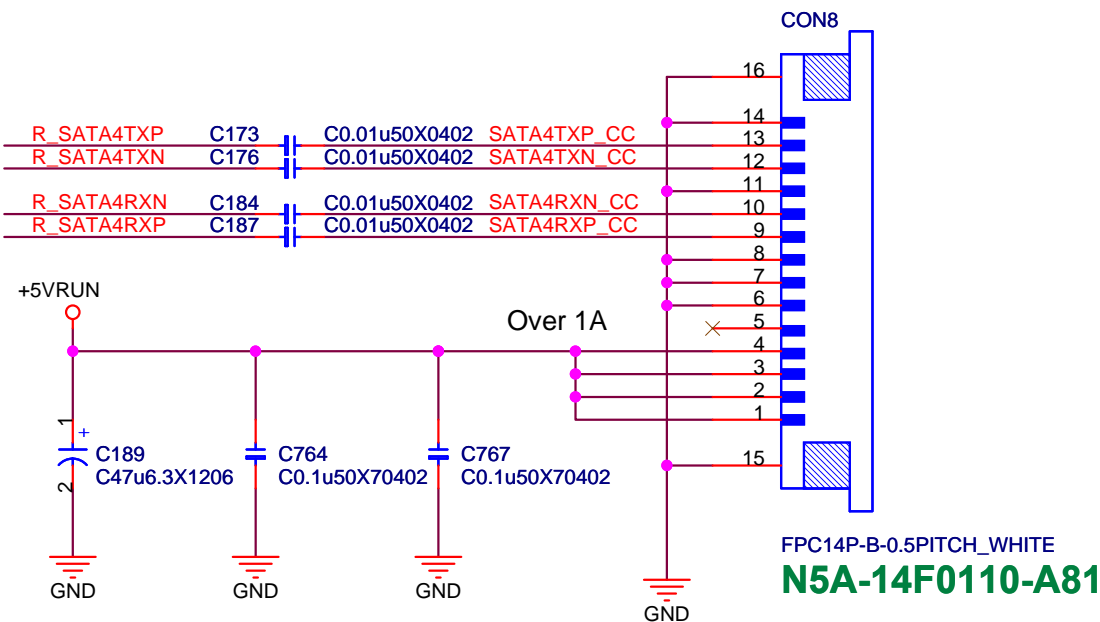
+3.3V LAN
(132mA)



HDD (With Repeater)



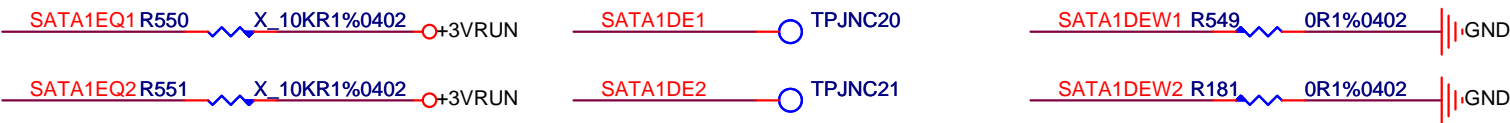
BTB Connector



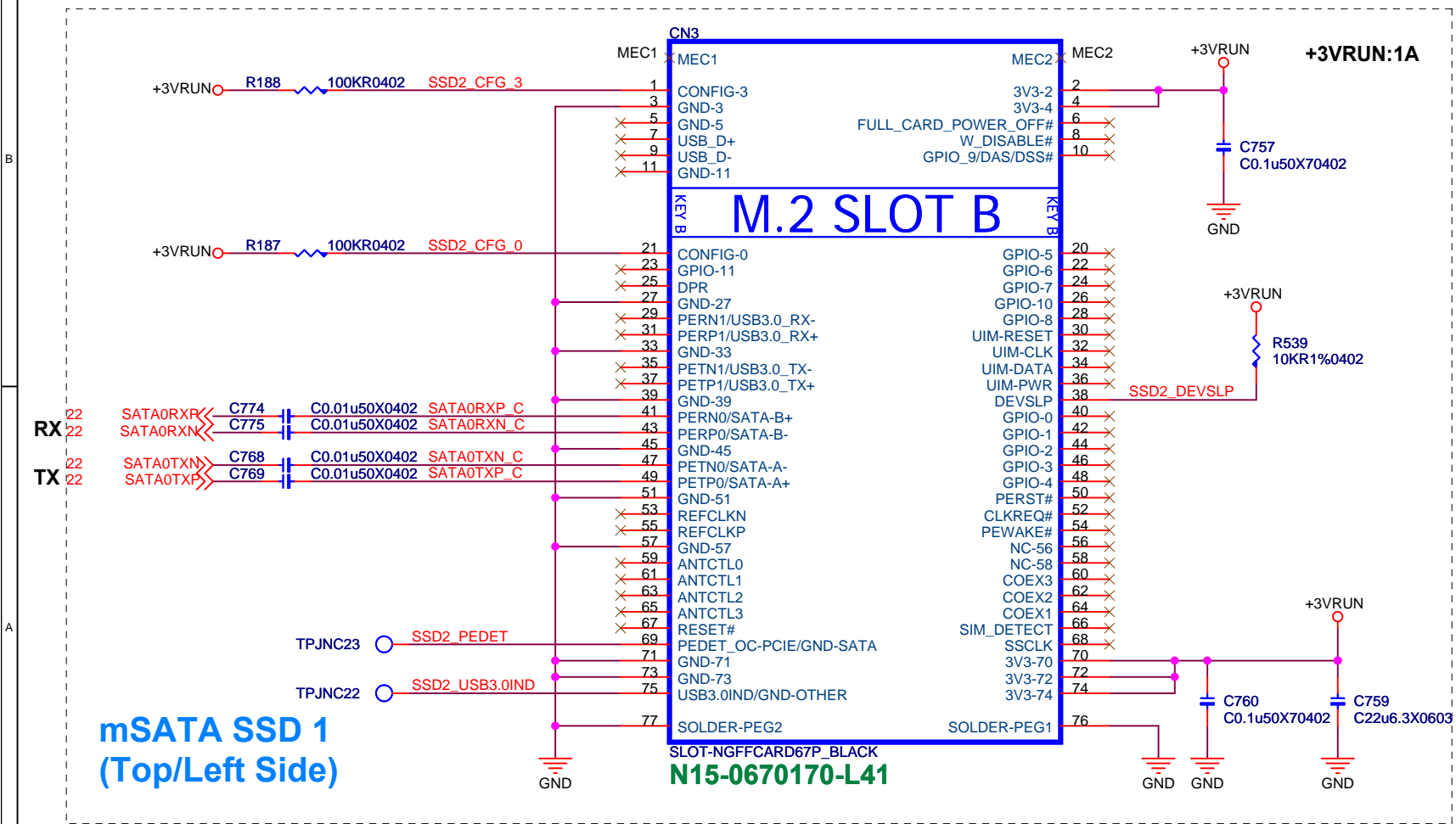
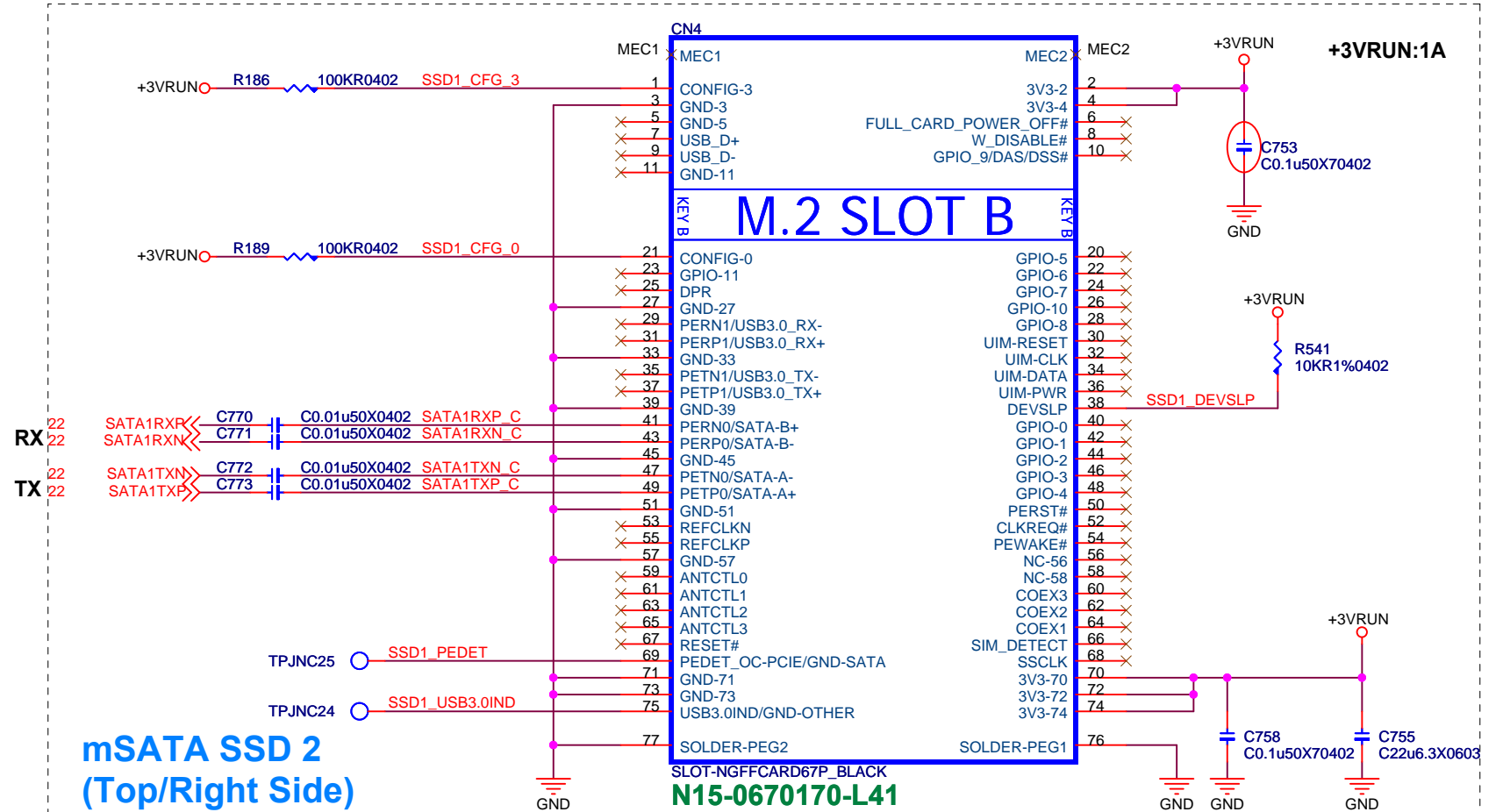
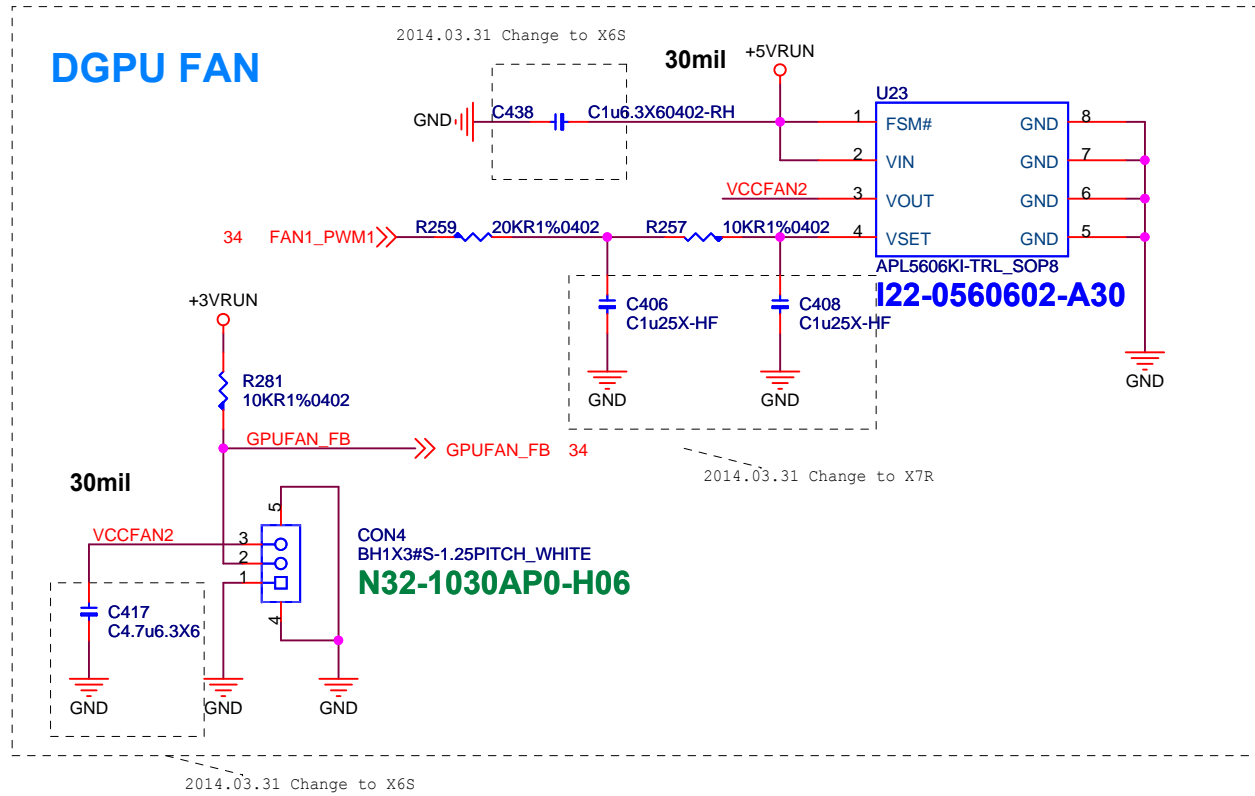
TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (<i>default</i>)	-4	NC (<i>default</i>)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (<i>default</i>)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)



SSD/ DGPU FAN



40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

[illegible]

Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

CAMERA

28 USB_P11N<<>> 3
28 USB_P11P<<>> 4

EL5
CMC-L12-9008084

For two vender on 1.0

34 CAMERA_ON# <<>> 1

GND EC41 C33p50N0402 EMI

20Mil FPC3

USB P11N R 8
USB P11P R 7
CAMERA_ON# 6
+5VRUN 5
+3VRUN 4
39 PDM_DATA_CONN 3
39 PDM_CLK_CONN 2

GND EC44 C33p50N0402 EMI Max (33pF+33ohm) EC43 C33p50N0402

BH1X8#S-1.25PITCH_WHITE
N32-1080730-H06

Close Connector

+3VRUN C460 C0.1u50X70402 GND

Click Pad

Same Side

TP_DATA_R
TP_CLK_R

ER4 0R1%0402
ER3 0R1%0402

R171 10KR1%0402
R170 10KR1%0402

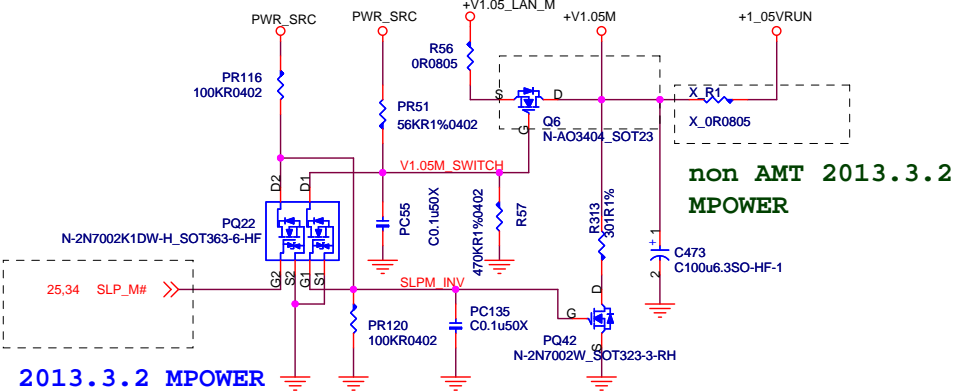
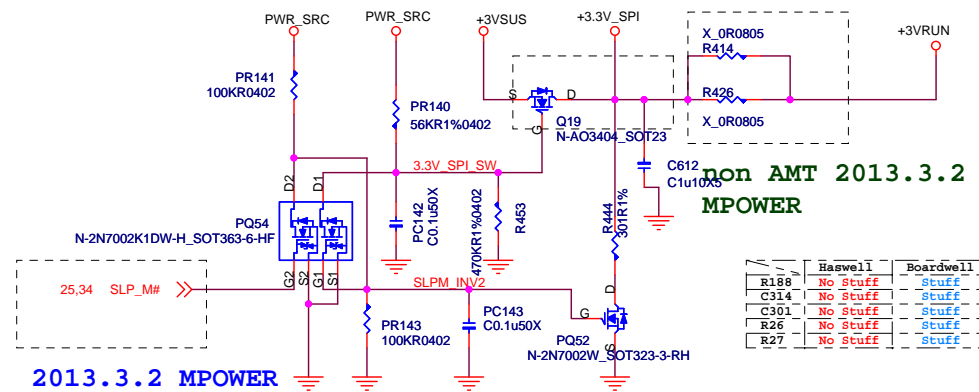
C83
X_C0.1u50X70402

+3V_RUN

EC34 X_C10p50N0402
EC33 X_C10p50N0402
EC68 X_C0.1u50X70402

FPC6
FPC6P-B-1PITCH_WHITE
N5A-06F0320-A81

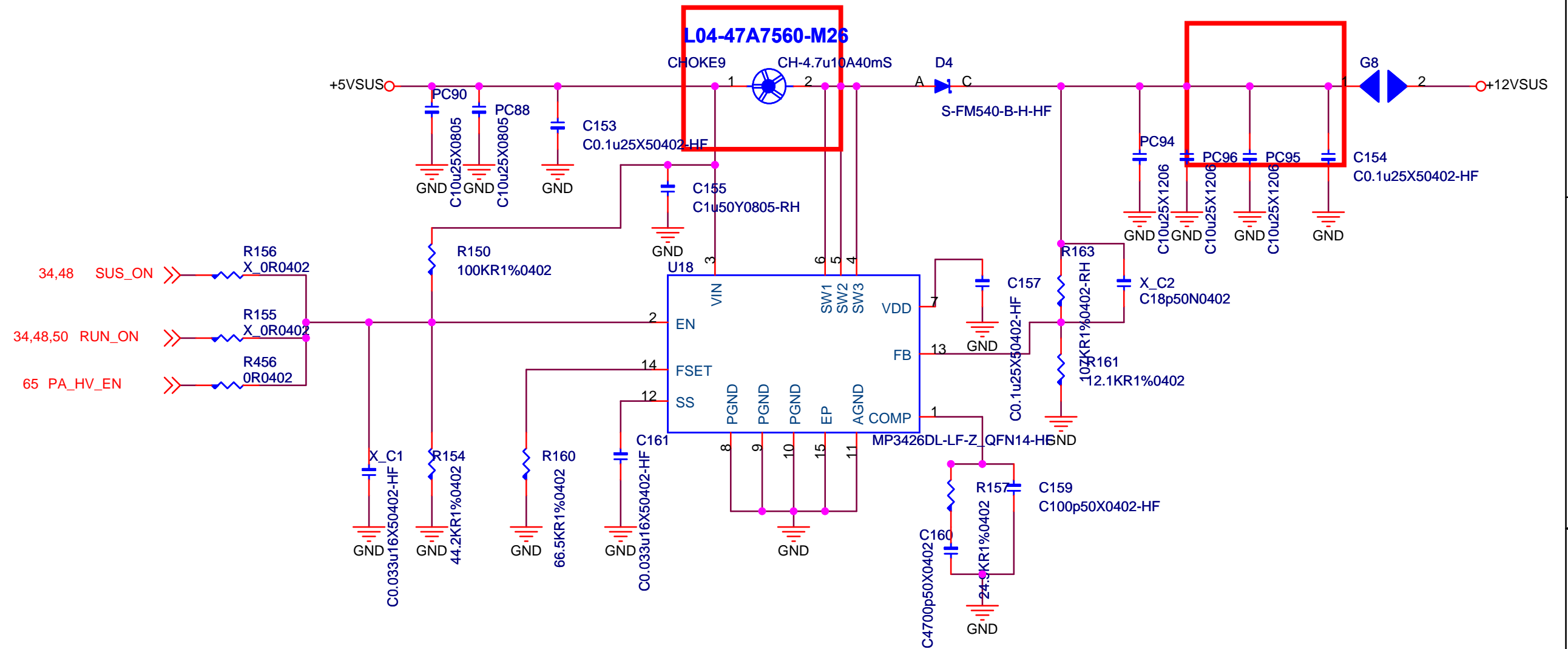
If Non-AMT, R267 stuff. This block no-stuff
If AMT, This block stuff, R267 no-stuff



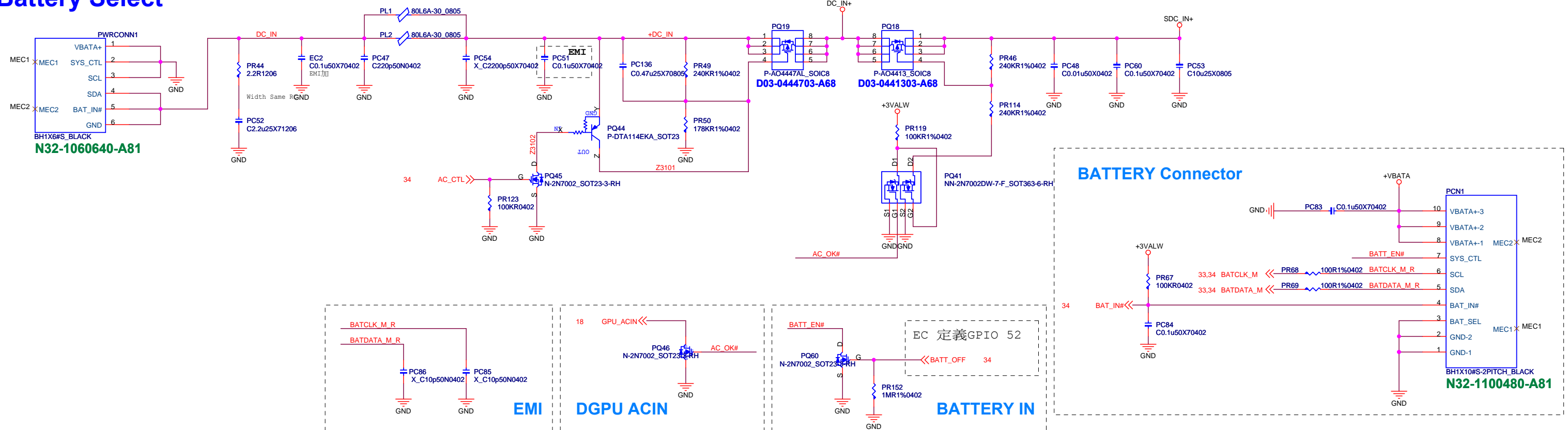
+1_05VRUN_PWRGD, AMT used

Schematic diagram of the +1_05VRUN_PWRGD signal path. The circuit includes a +1_05VRUN input, a +3VSUS input, and a +3VSUS input. The +1_05VRUN input is connected to a 30.1K/4/1 resistor (R30) and a 30.1K/4/1 resistor (R31). The +3VSUS input is connected to a 33K/4/1 resistor (R26) and a 33K/4/1 resistor (R28). The output of the circuit is +1_05VRUN_PWRGD. The circuit also includes a 30.1K/4/1 resistor (Q82), a 30.1K/4/1 resistor (B2), a 30.1K/4/1 resistor (C67), a 0.1uF/X7R16V/4 capacitor (C64), and a 0.1uF/X7R16V/4 capacitor (C67). The circuit is labeled NN-CMKT3904_SOT363-6-RH.

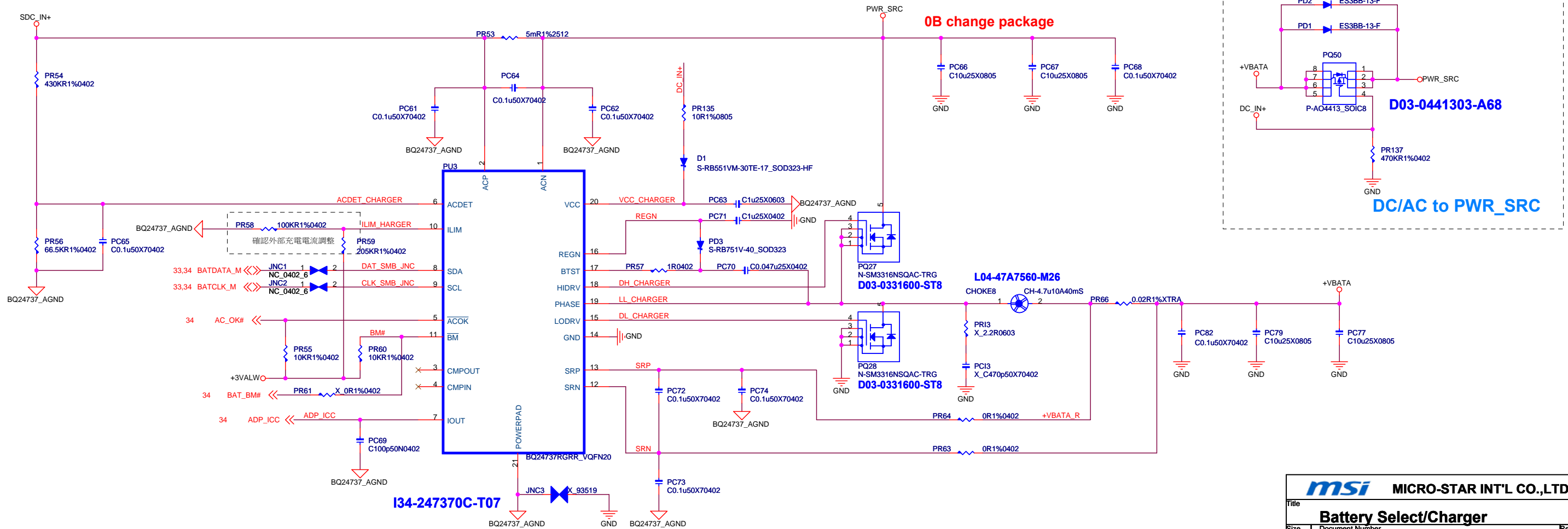
TBT Power 5V Boost 12V 1A



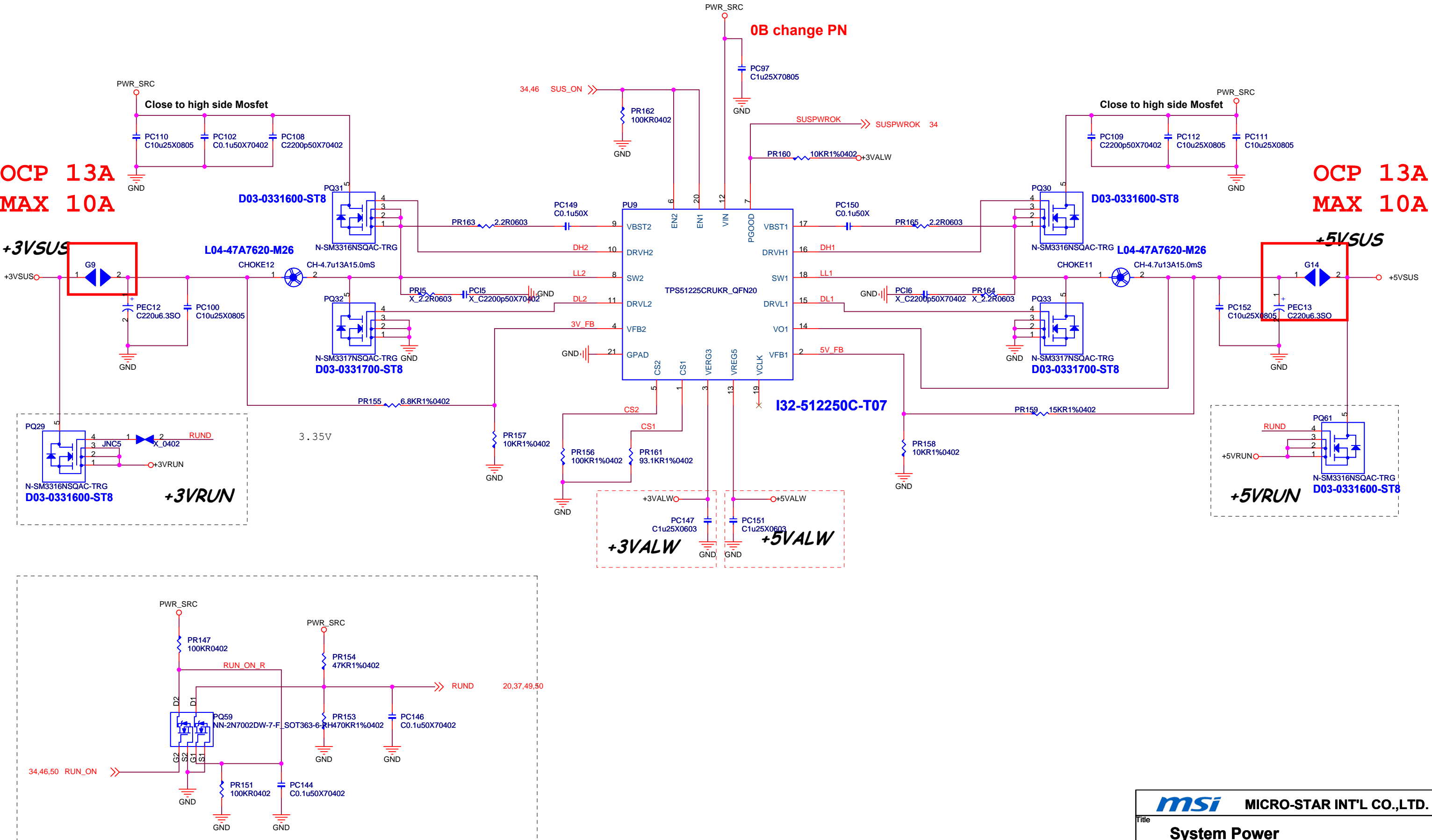
Battery Select



Battery Charger

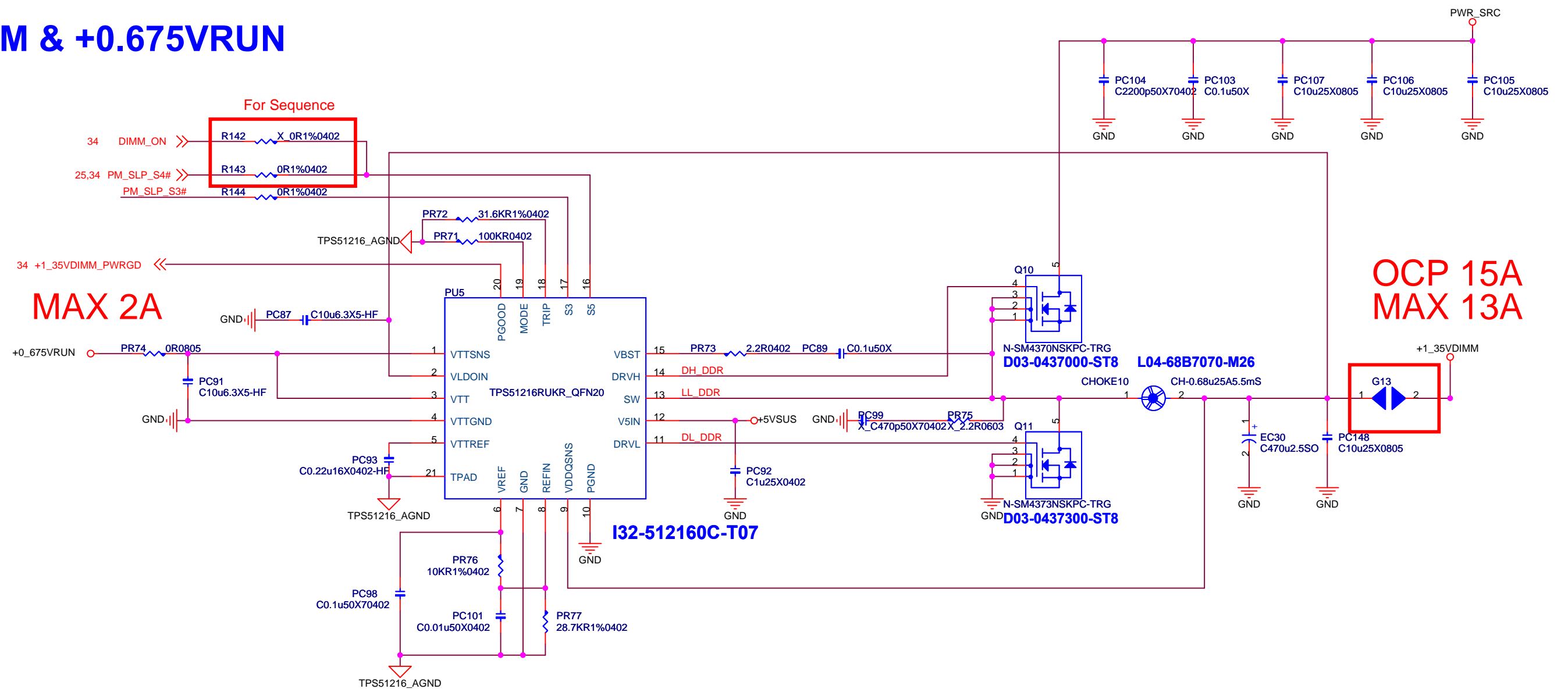


System Power

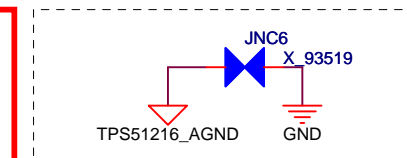
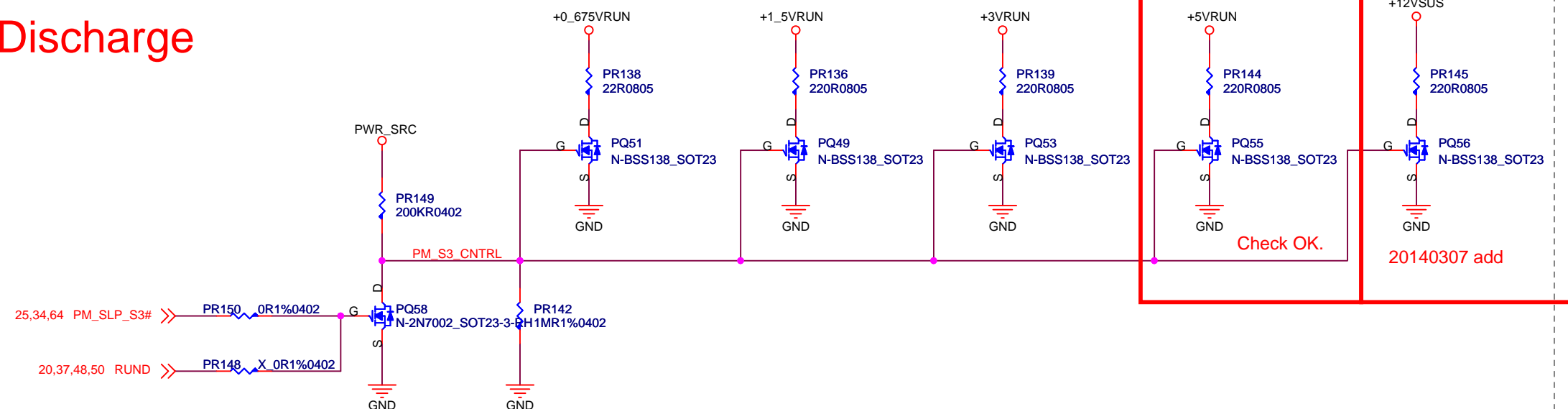


+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN



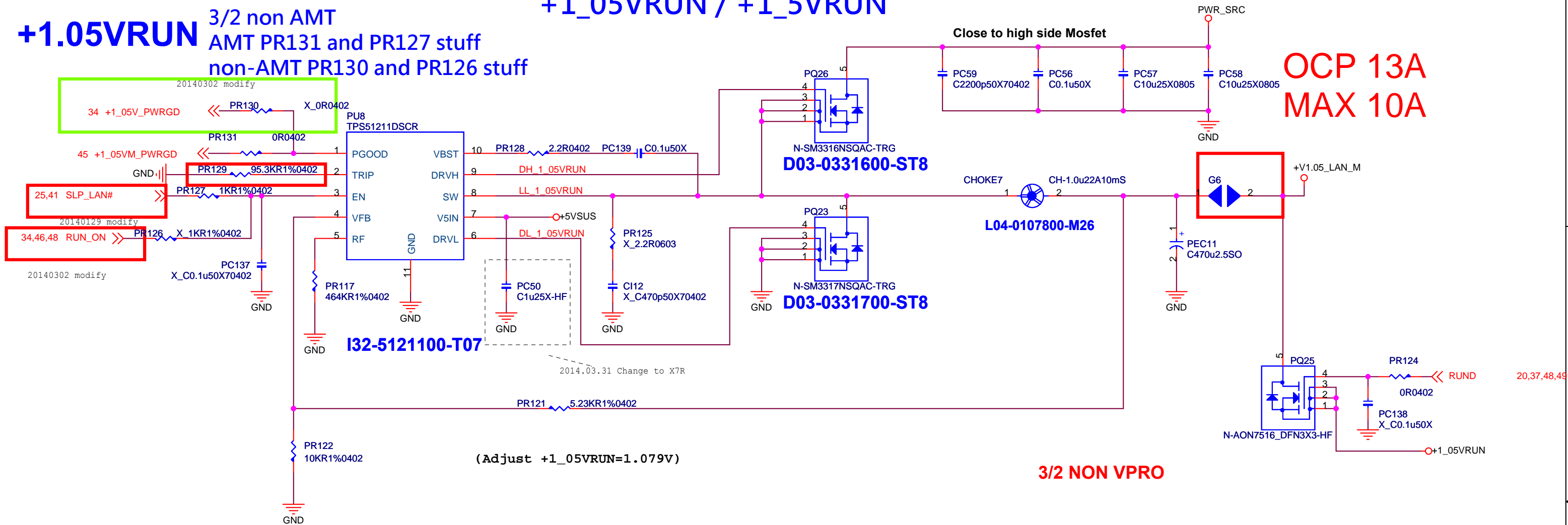
Discharge



+1.05VRUN 3/2 non AMT AMT PR131 and PR127 stuff non-AMT PR130 and PR126 stuff

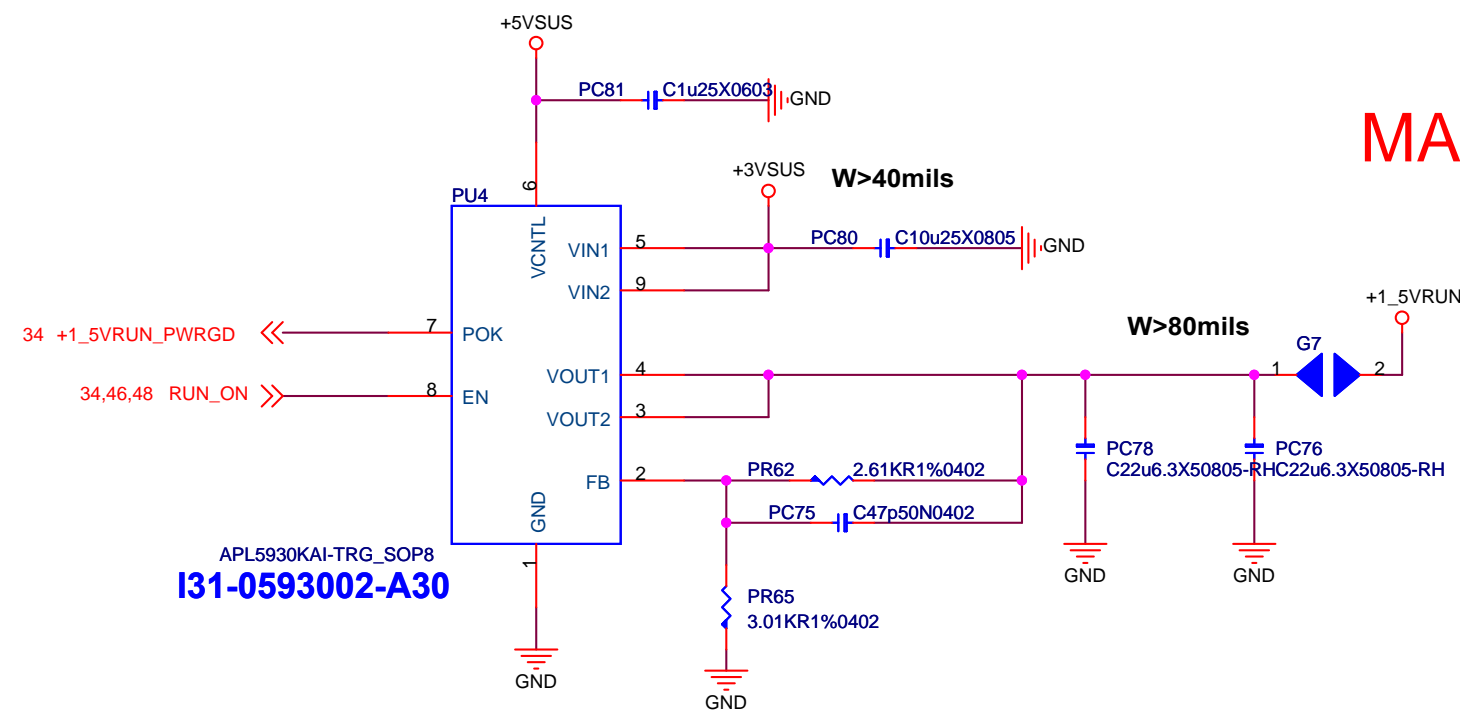
+1_05VRUN / +1_5VRUN

**OCP 13A
 MAX 10A**



+1.5VRUN

MAX 2A

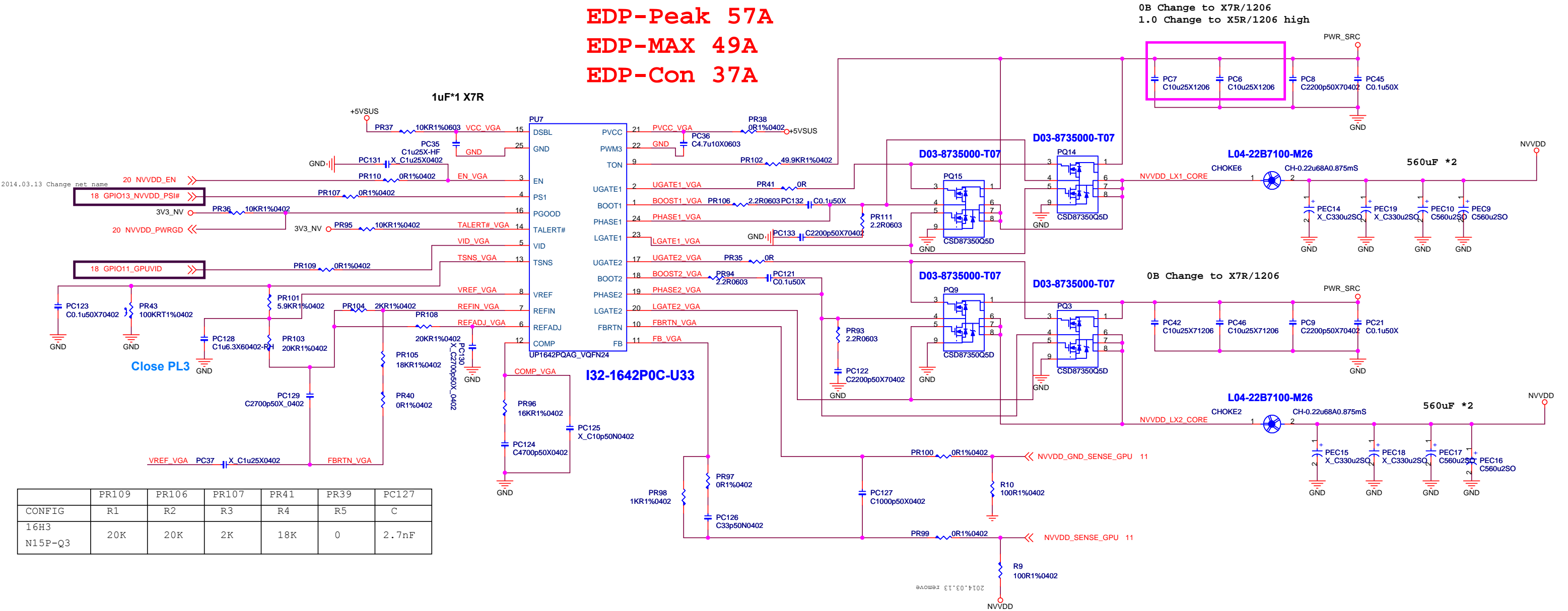


DGPU POWER NVVDD

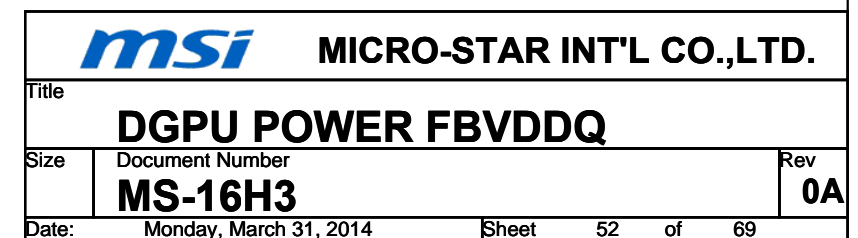
DGPU POWER / UP1642PQAG

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 57A
EDP-MAX 49A
EDP-Con 37A



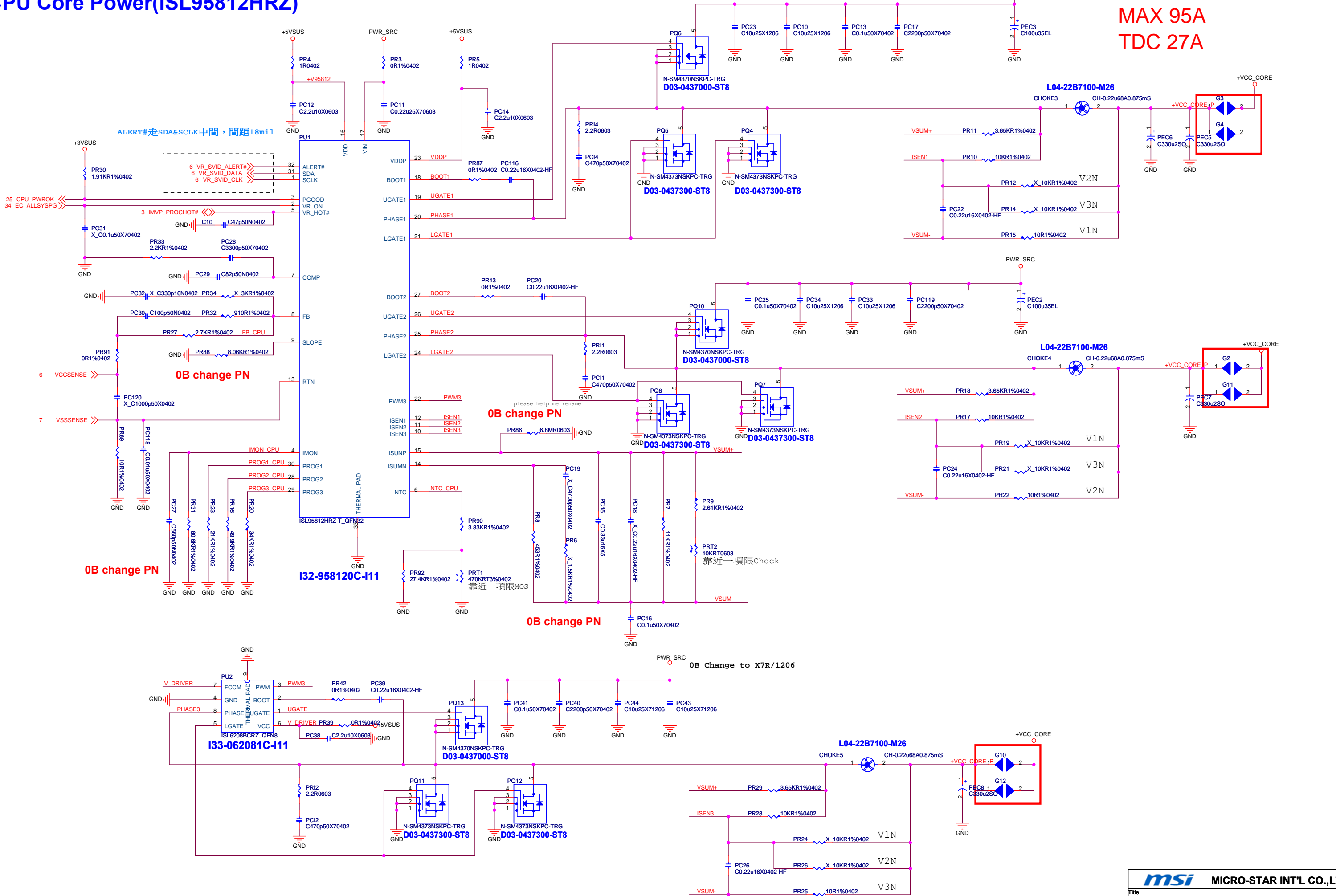
FBVDDQ



CPU Core Power(ISL95812HRZ)

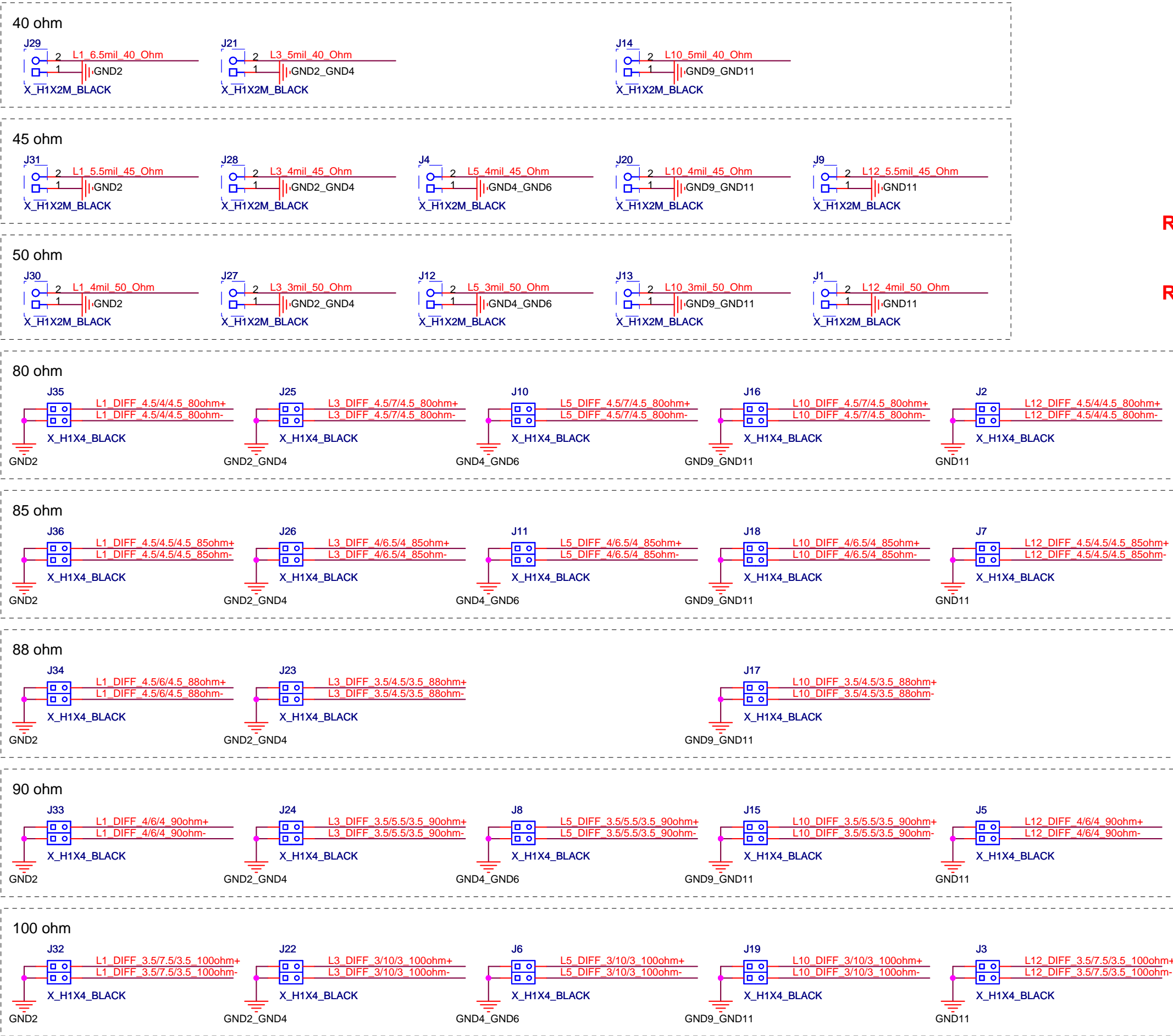
CPU Power (+VCC_CORE)

MAX 95A
TDC 27A

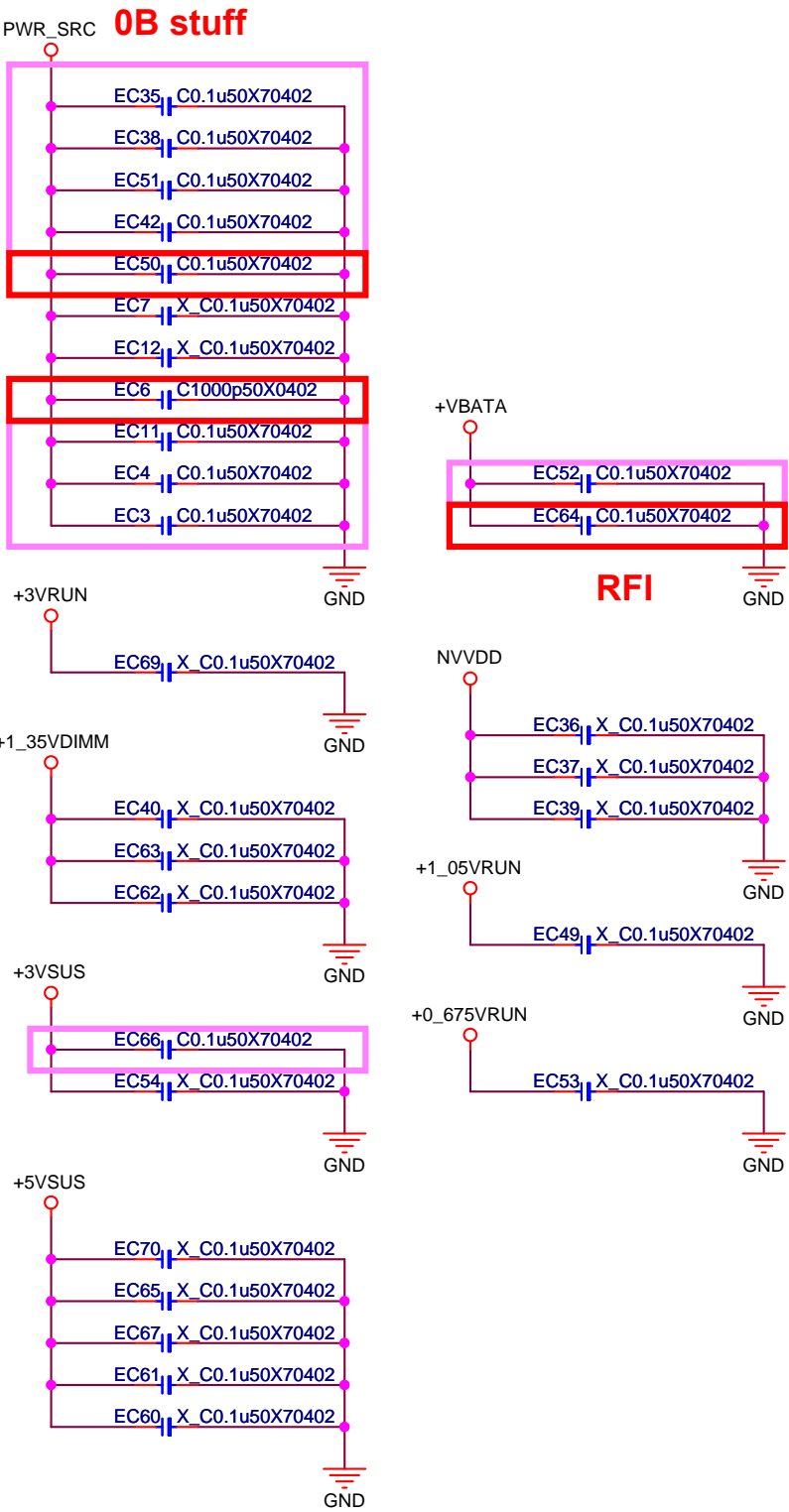


EMI/ Impedence

Impedence Connector No PN

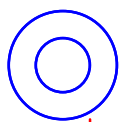


EMI

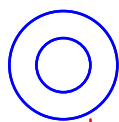


CPU/GPU Holes

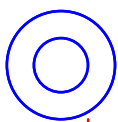
MCPU4
H_R200D150



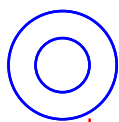
MCPU2
H_R200D150



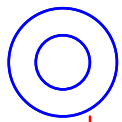
MCPU3
H_R200D150



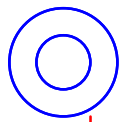
MCPU1
H_R200D150



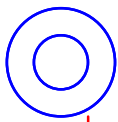
MGPU2
H_R276D169_PB



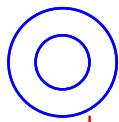
MGPU4
H_R276D169_PB



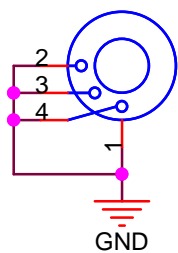
MGPU1
H_R276D169_PB



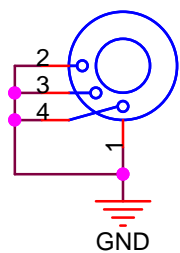
MGPU3
H_R276D169_PB



M1
X_H_R197D118_PT_V3
H_R197D118_PT_V3



M6
X_H_R197D118_PT_V3
H_R197D118_PT_V3



EMI

SPRING3
X_MECHCU,2.5*5.5*0.1mm

SPRING2
X_E2M-7213211-RH



GND
E2M-7213211-CA7

SPRING1
X_E23-1029060-RH



GND
E2M-2142011-CA7

SPRING1
X_E23-1029060-RH



GND
E23-1029060-CA7

SPRING4
X_E2M-7213211-RH



GND
E2M-7213211-CA7

MYLAR2



E2P-6H23111-Y42

MYLAR

MYLAR3



E2P-6H22711-Y42

MYLAR

RUBBER1



E2Y-6H20712-Y40

RUBBER

RUBBER2



E2Y-6H21312-Y40

RUBBER

RUBBER3



E2Y-6H21312-Y40

RUBBER

BRACKET1



307-6H20111-C22

CPU_BRACKET

BRACKET2



307-6H20111-C22

CPU_BRACKET

BRACKET3



307-6H20211-C22

GPU_BRACKET

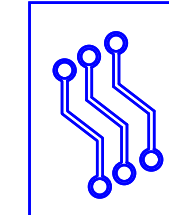
MYLAR1



E2P-6H22111-Y42

MYLAR

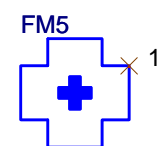
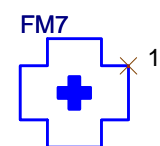
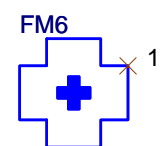
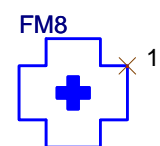
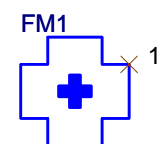
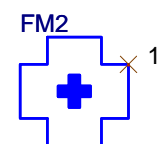
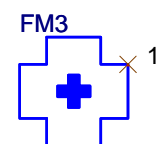
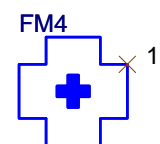
PCB1



PF0-16H3110-H73

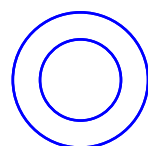
PF0-16H310A-H73

Hannstar: PF0-16H2110-H73
TRIPOD: PF0-16H2110-T53



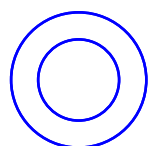
Fan Hole

MH4
H_R197D91
X_ME_SCREW HOLE

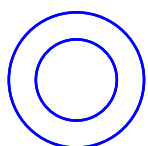


SSD Stand off

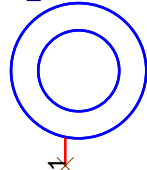
MH2
H_R220D146_PTB
E2B-16H2020



MH1
H_R220D146_PTB
E2B-16H2020



MH3
NPTH157
X_NPTH157



UME1



X_HDMI ROYALTY

Y01-RHDMI03-000 G51-LA01678-A09

For MP

UME2



X_BIOS_LABEL

Y01-RHDMI03-000 G51-LA01678-A09

For MP

msi

MICRO-STAR INT'L CO.,LTD.

Title

Screw/ME

Size

Document Number

MS-16H3

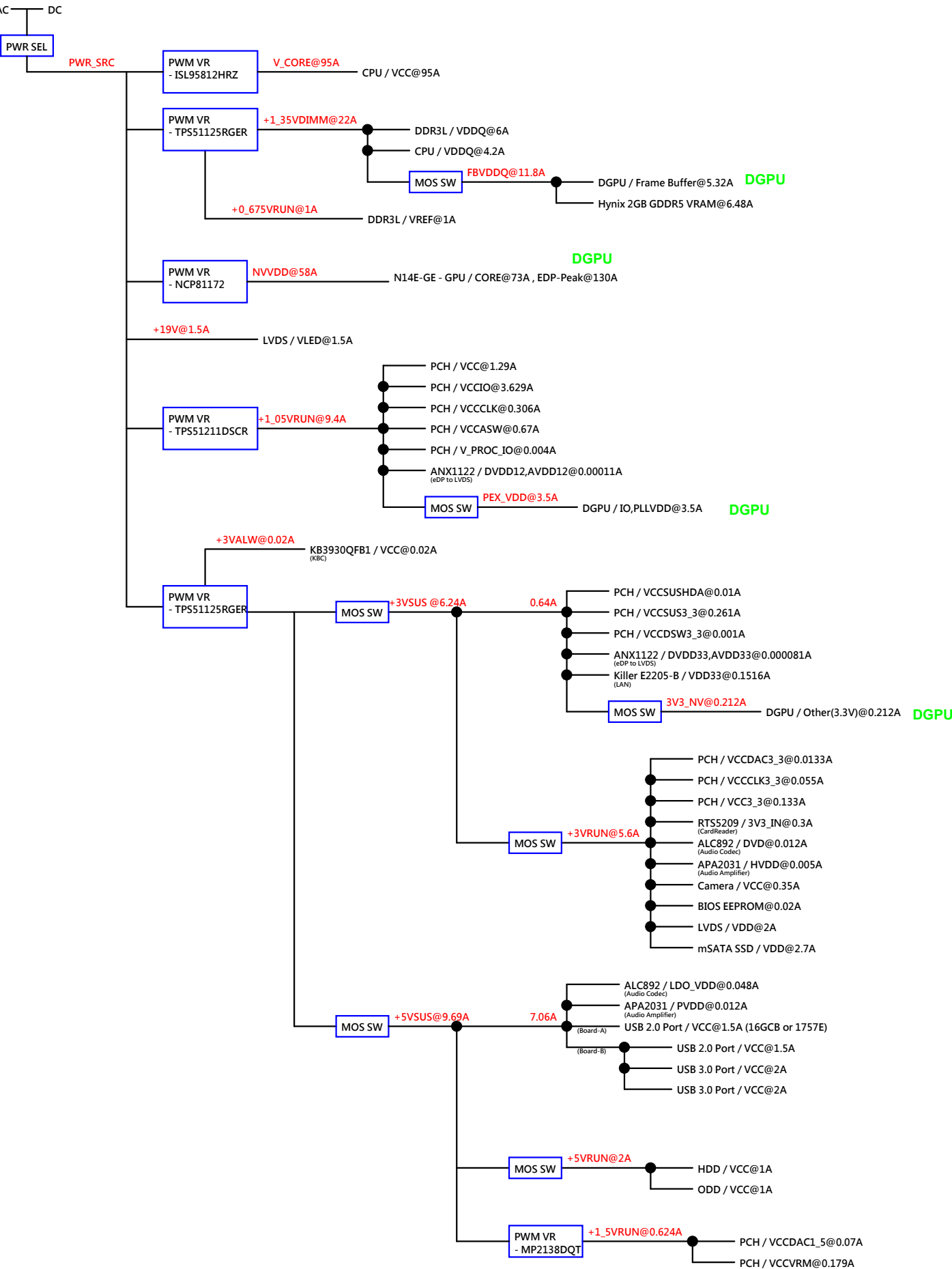
Rev

0A

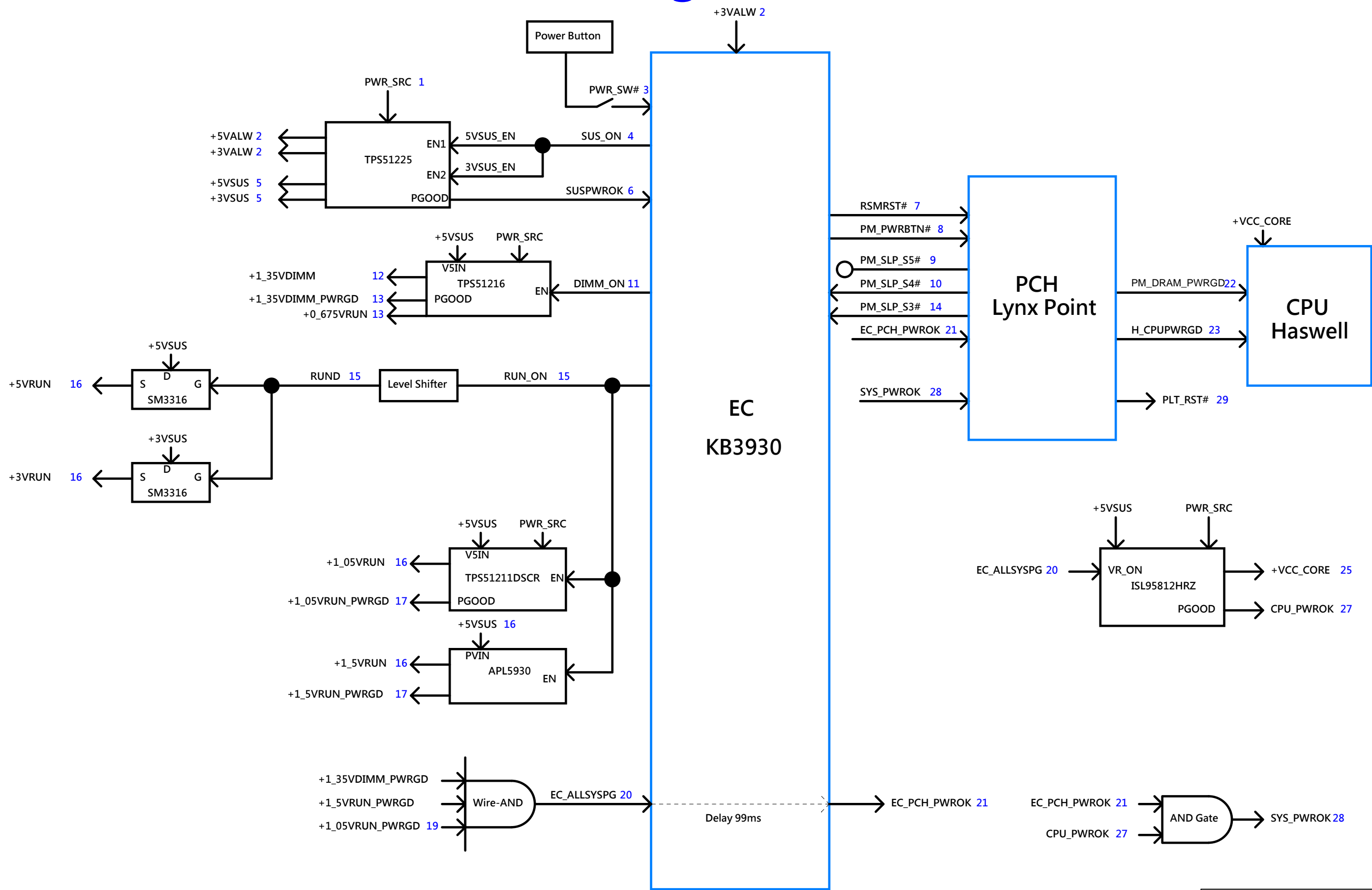
Date: Tuesday, April 01, 2014

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MS-16H2 Power Delivery Chart

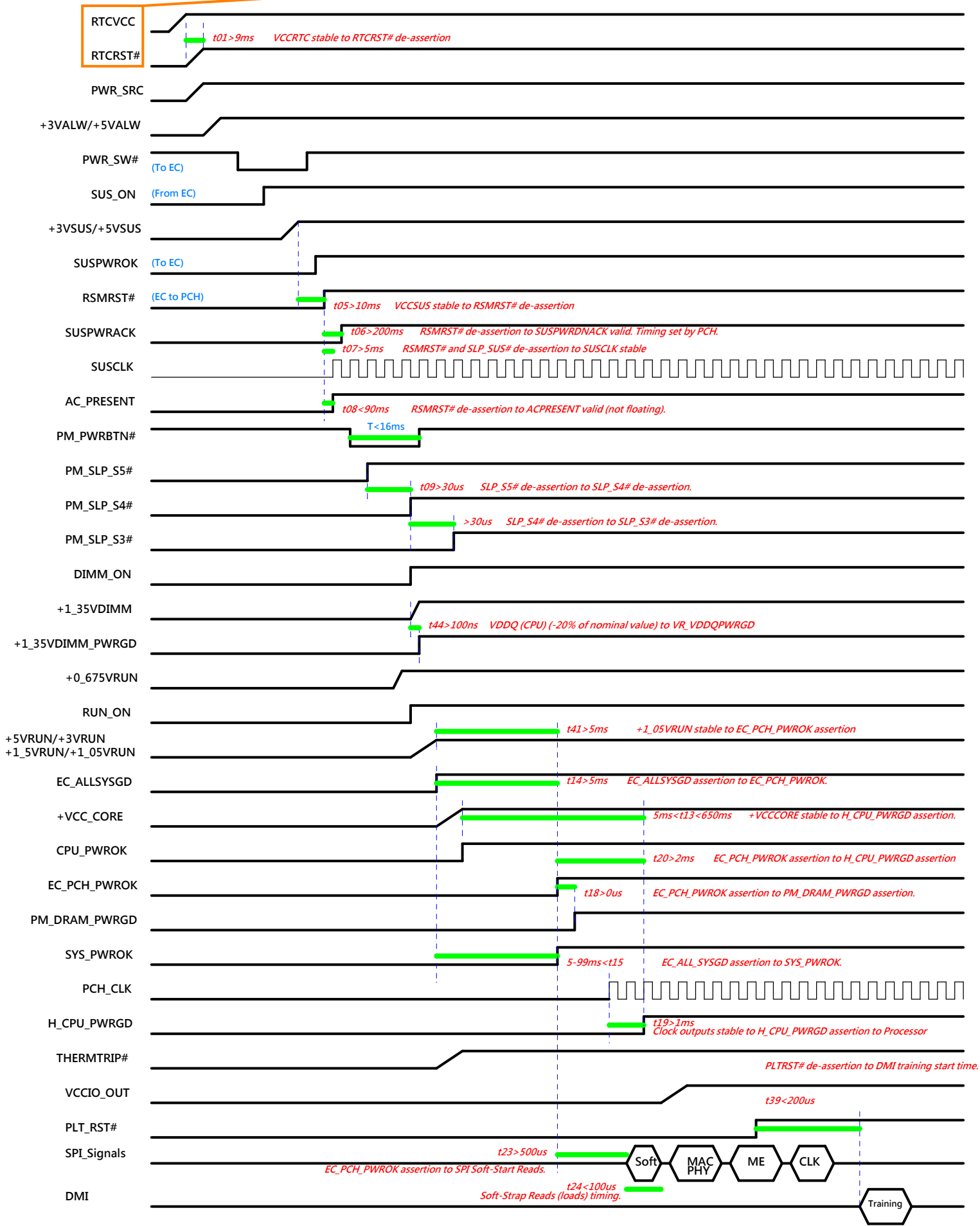


MS-16H2 Power on Block Diagram

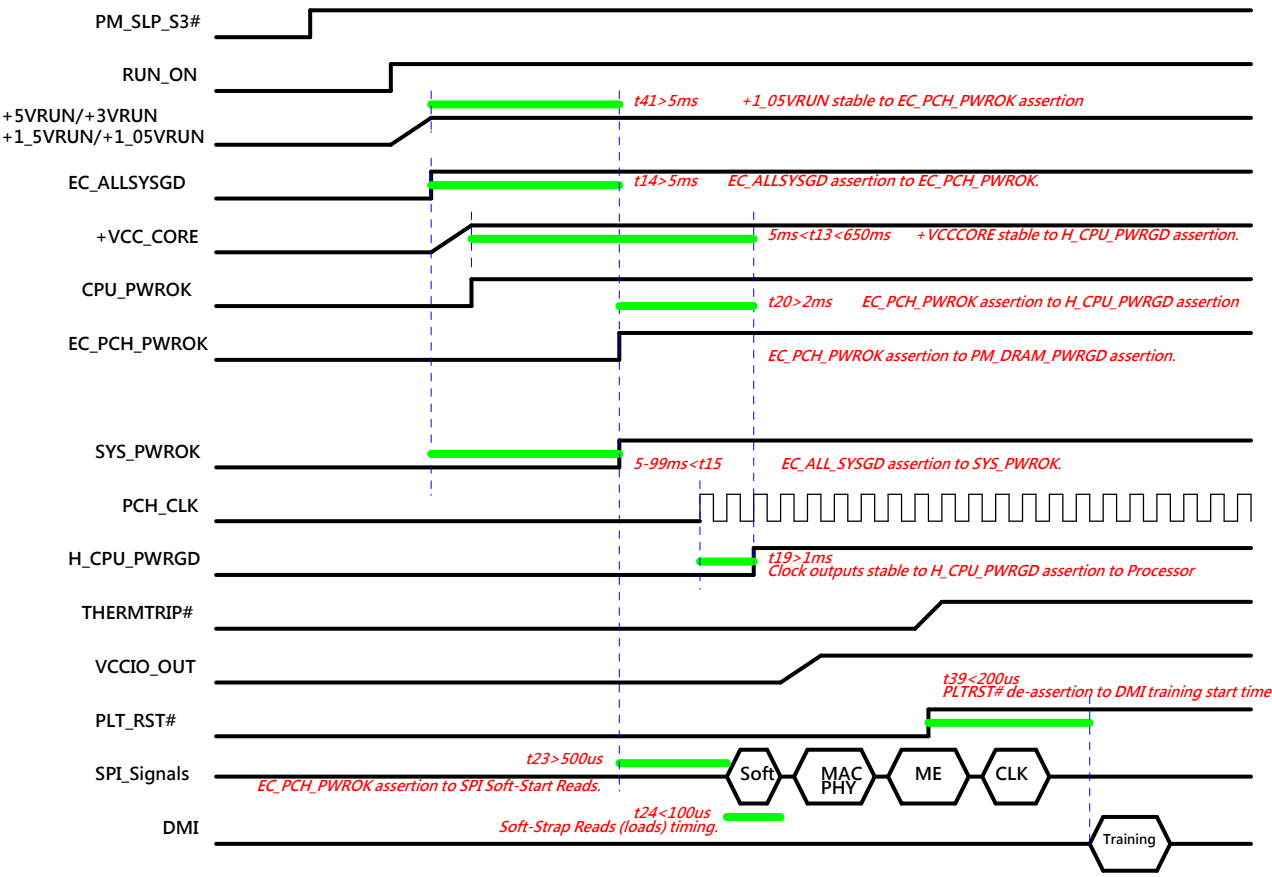


Power on Sequence

G3 -> S0

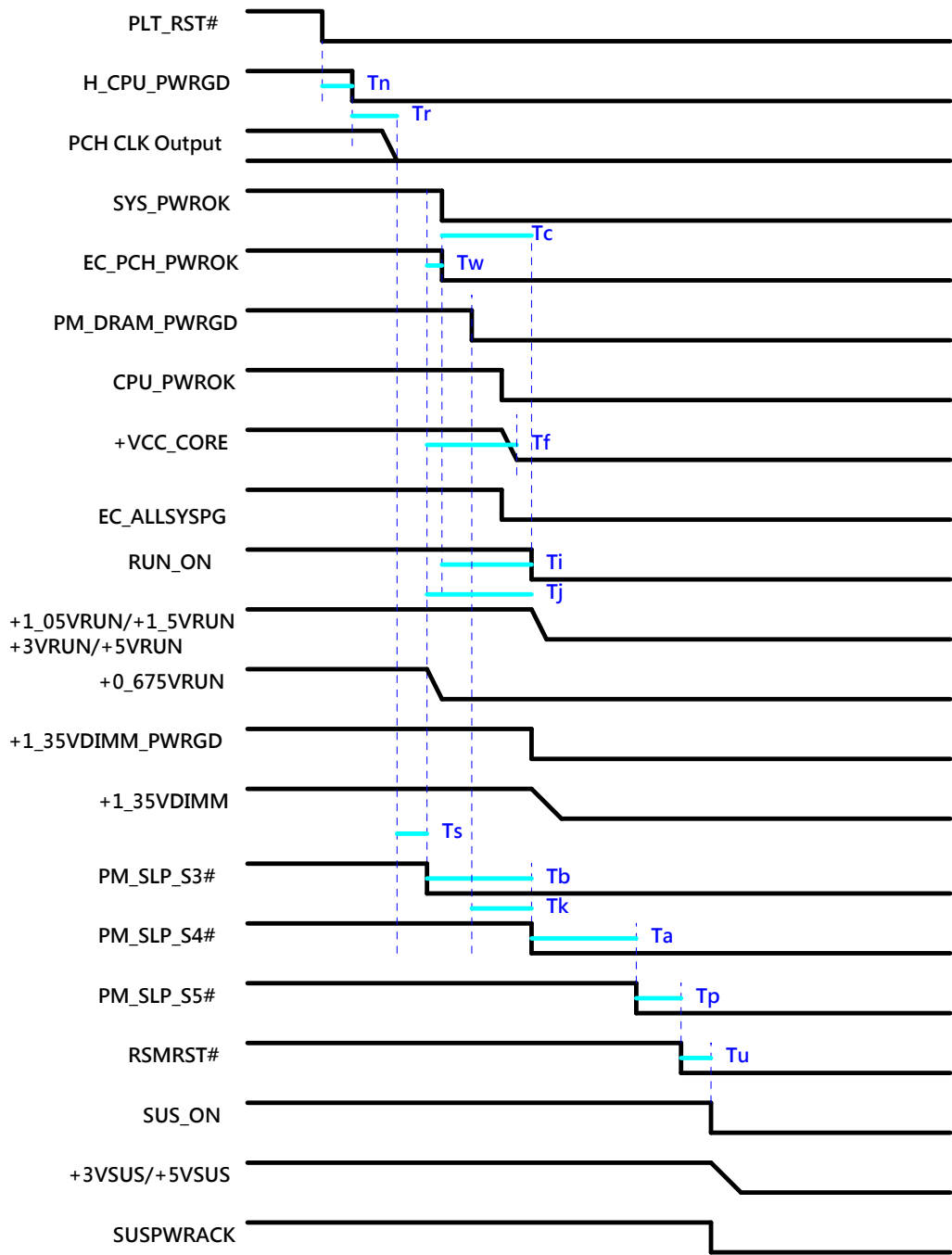


S3-> S0



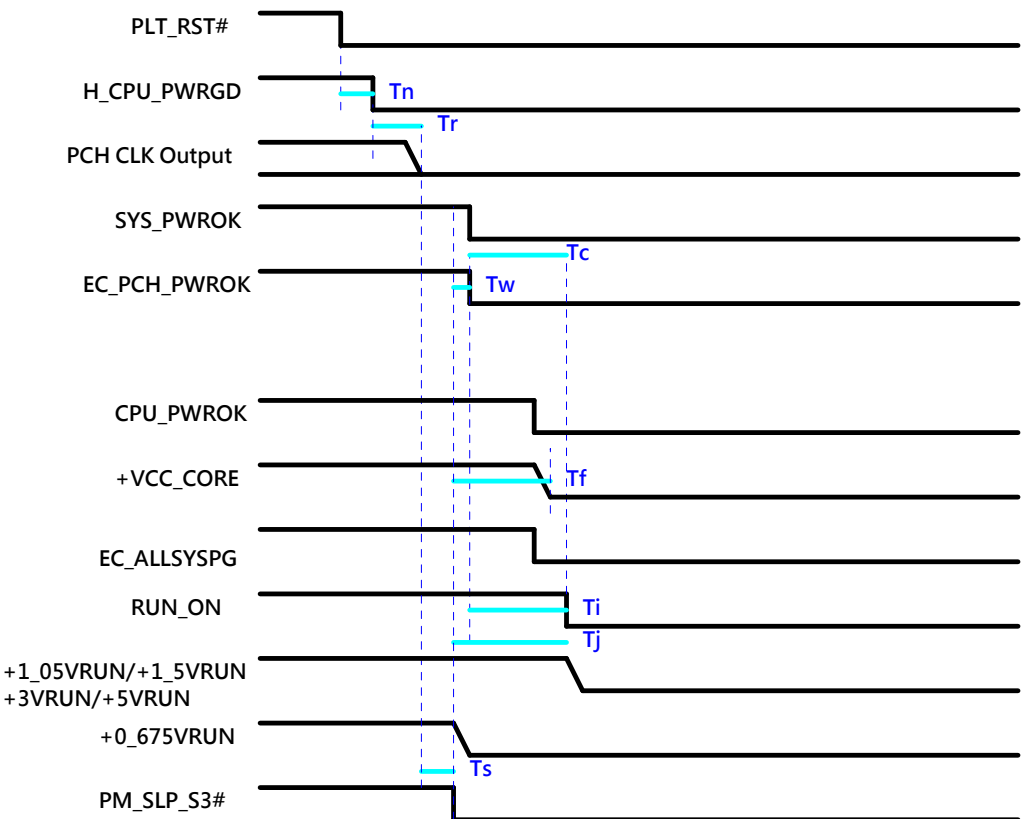
Power down Sequence

S0 -> G3

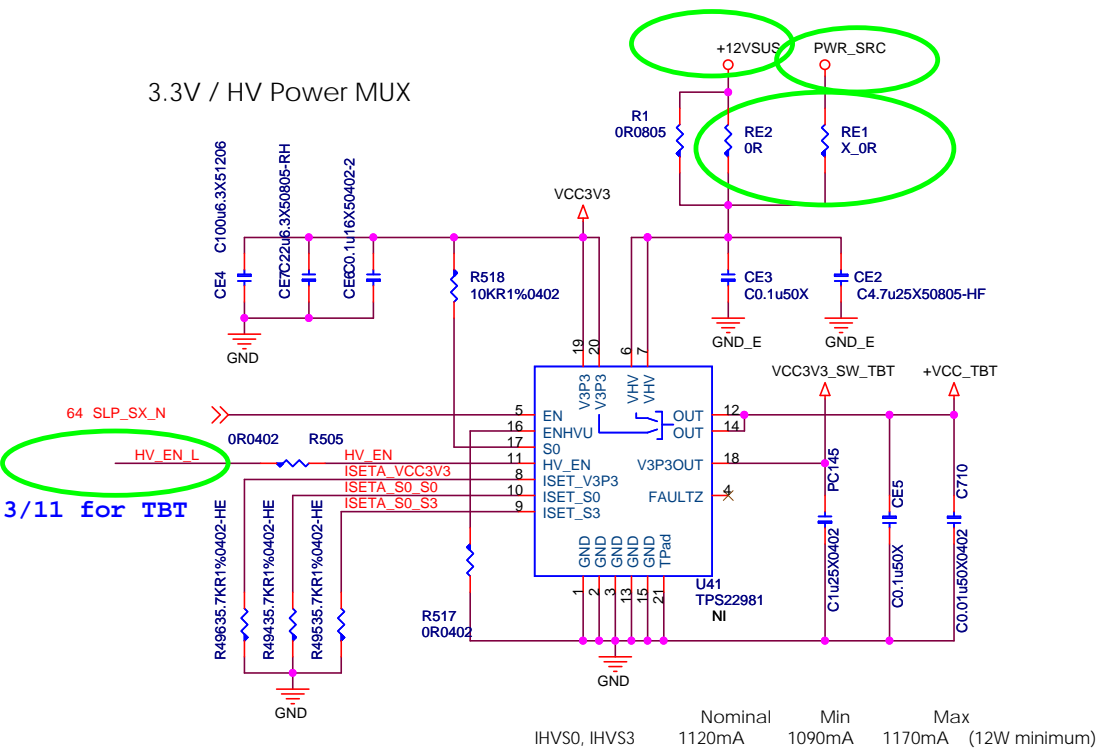


	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

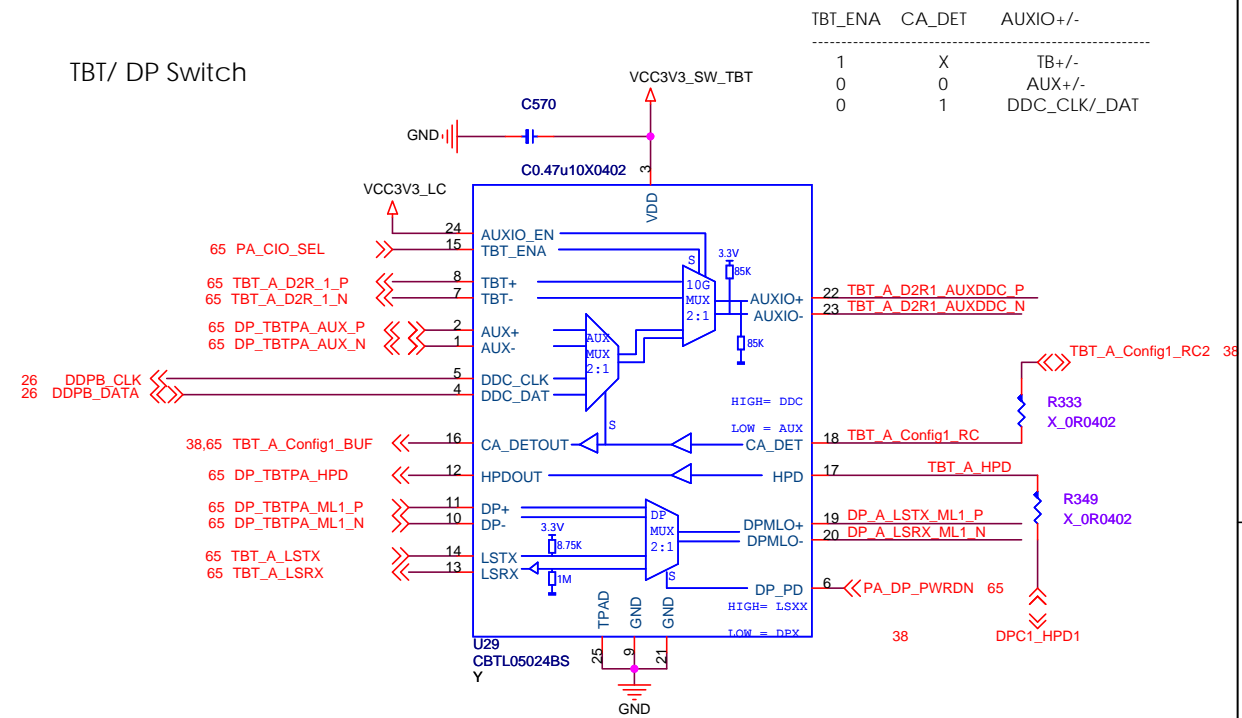
S0 -> S3



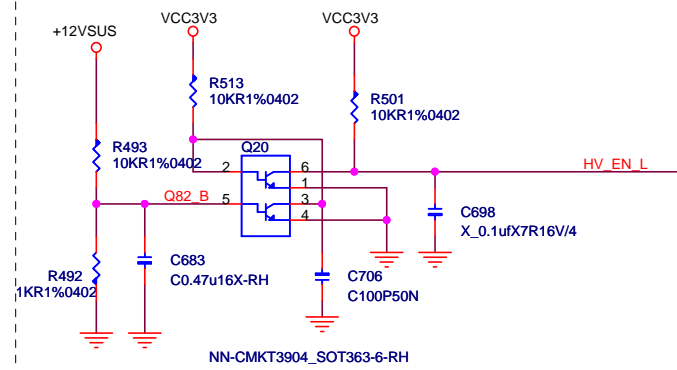
3.3V / HV Power MUX



TBT/ DP Switch

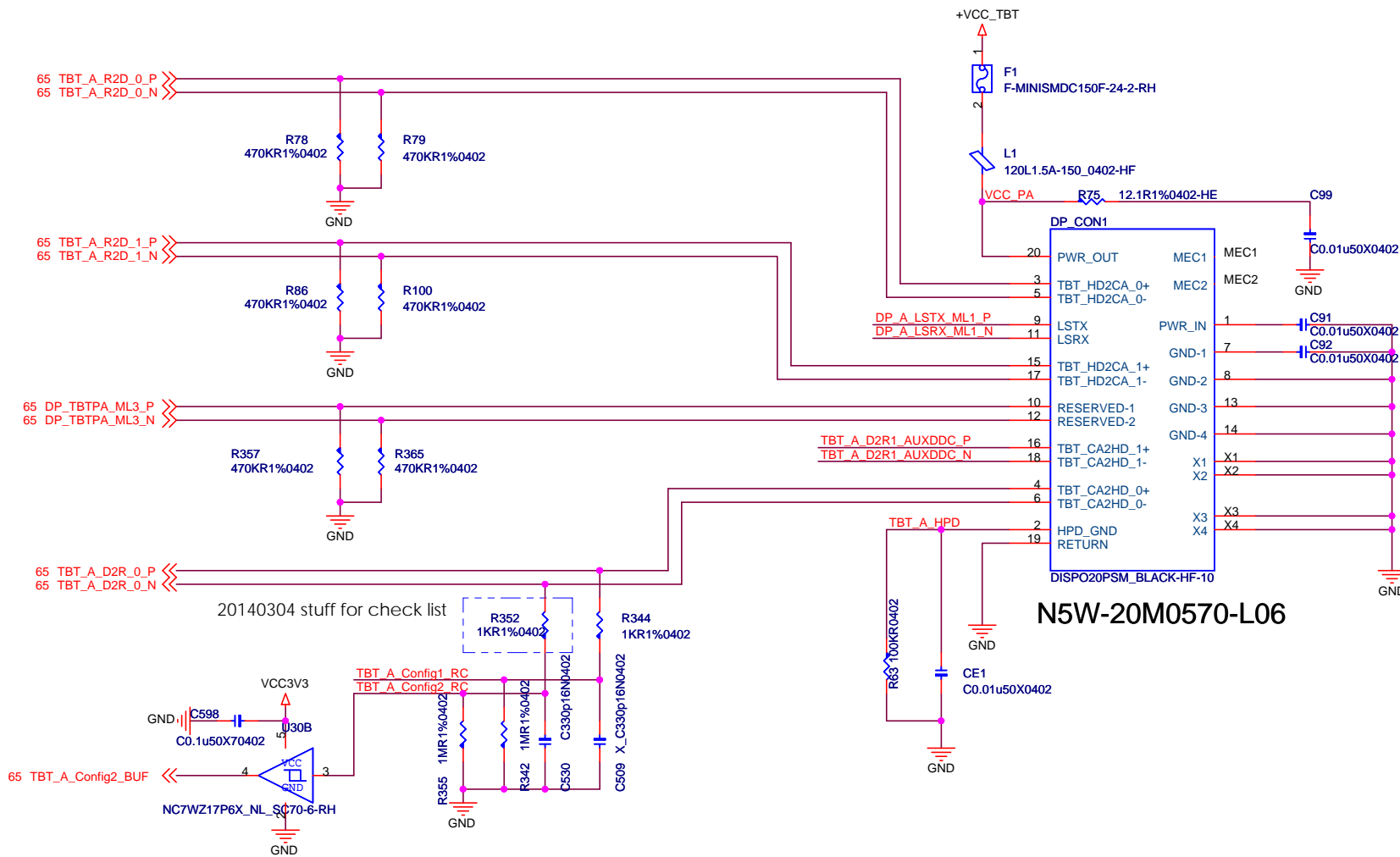


3/11 for TBT



Power mux will be
on when VCC12V0 >=4.5V and
off when VCC12V0 <=3.4V
Vbe=770mV@Ic=10mA -->
 $4.5 \times 2.05K / (10K + 2.05K) = 0.766V$

Note:
If generating the 12v from a supply different than 3.3v - resistors values of R52 and R53 should be different
Example: If VCC12V0 is boosted from 5V, the R52 is 10K ohm and R53 is 1K ohm



History

0B: Hardware part

- 01. Remove All GAP for power parts.
- 02. Add 3V3_NV part for leakage
- 03. Change cardreader PN.
- 04. Change BTB PN
- 05. Change SPDIF/ Audio Jack PN
- 06. R116 unstuff, R117 stuff.
- 07. R346 unstuff
- 08. Remove SUBWOOFER
- 09. Add one more AMP for SPK

0B: Power part

- 01. PR33 2.2Kohm R11-0222T12-W08
- 02. PC29 82pF/50V C11-8201012-W08
- 03. PC30 100pF/16V C11-1011032-W08
- 04. PR34 unstuff
- 05. PC32 unstuff
- 06. PR27 2.7Kohm R11-0272T12-W08
- 07. PR90 8.06Kohm R11-8061T12-W08
- 08. PR32 910Rohm R11-0911T12-W08
- 09. PC27 560pF/16V C11-5611812-W08
- 10. PR31 80.6Kohm R11-8062T12-W08
- 11. PR23 21Kohm R11-0213T12-W08
- 12. PR88 6.8Mohm R11-0685T13-W08
- 13. PR8 453Rohm R11-4530T22-W08
- 14. PC19 unstuff
- 15. PR6 unstuff
- 16. PR140 100Kohm R11-0104T12-W08
- 17. PR145 93.1Kohm R11-9312T12-R01
- 18. PR143 15Kohm R11-0153T12-W08
- 19. PR124 95.3Kohm R11-9532T12-W08
- 20. PR86 28.7Kohm R11-2872T12-W08
- 21. PC69, PC70 change to 1206 package
- 22. PR88 6.8Mohm R11-0685T13-W08